

Compal Confidential

FH50P MB Schematics Document

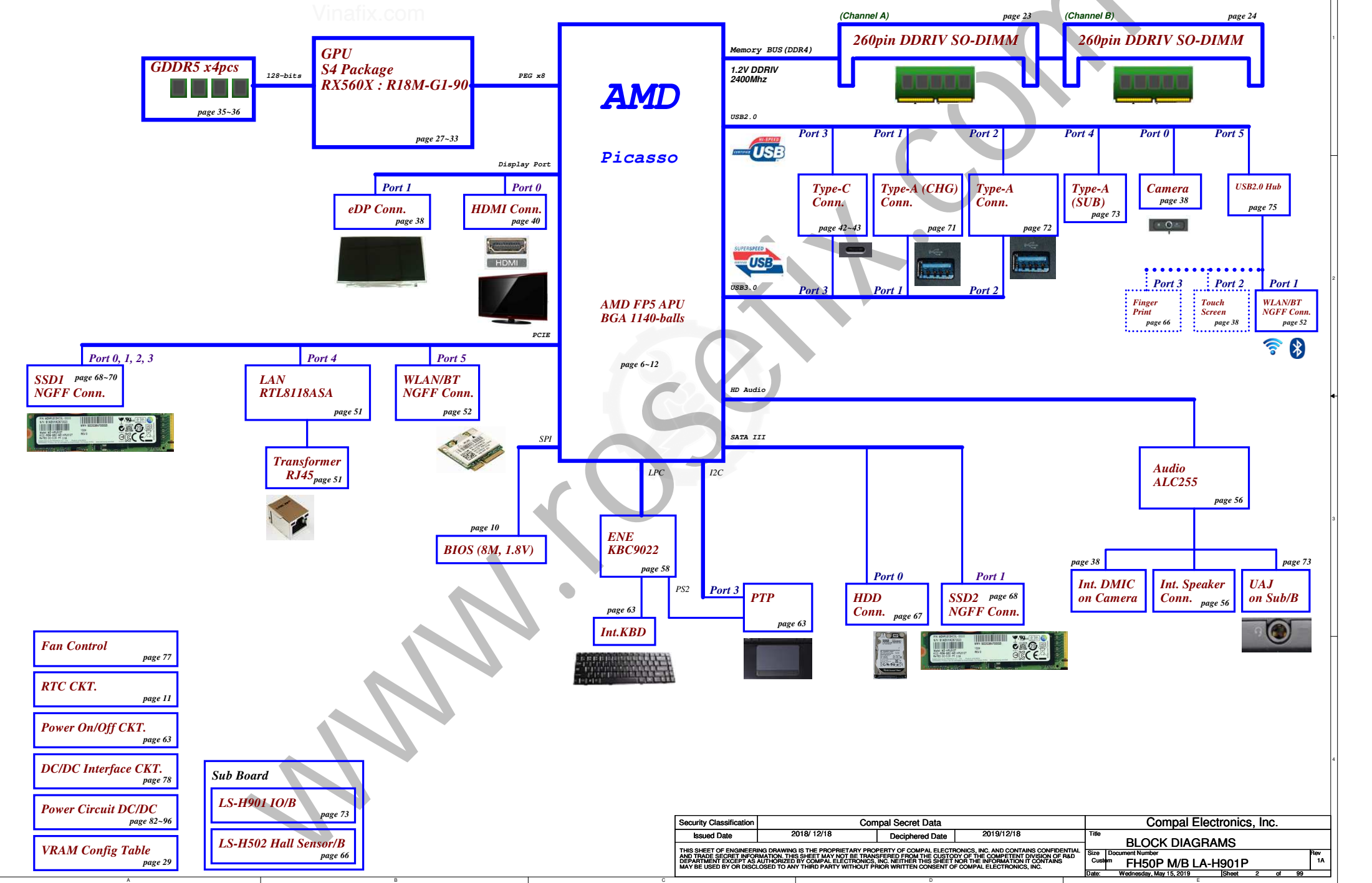
AMD Picasso Platform

AMD R18M-G1-90

LA-H901P REV:1A

2019-05-13

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Voltage Rails

Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)				
I2C Port 2 (+3VS)				
SBMUS Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC SMBus Address Table

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TS1)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h
	Thermal Sensor (Remote1 GPU) (Remote2 APU)		1001 1010b 9Ah	1001 1011b 9Bh
SMBus Port 3 (+3VALW)	LED driver		1100 0000b C0h	1100 0001b C1h

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	PVT
2	MP
9	With RGB BL

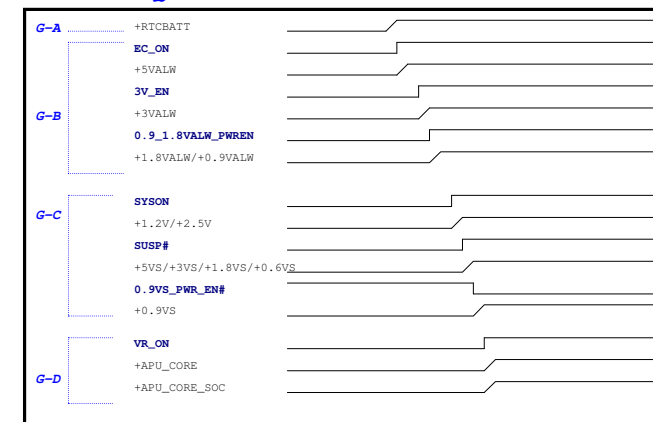
BOM Structure Table

[illegible]

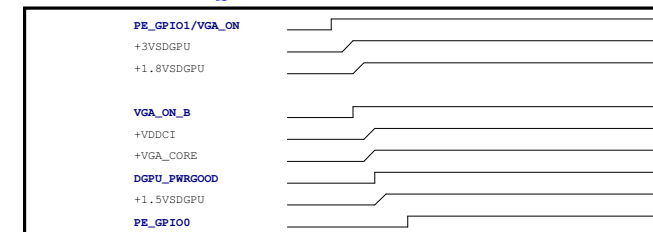
Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE
19	NC	3.000V	3.300V		0xEF - 0xFF

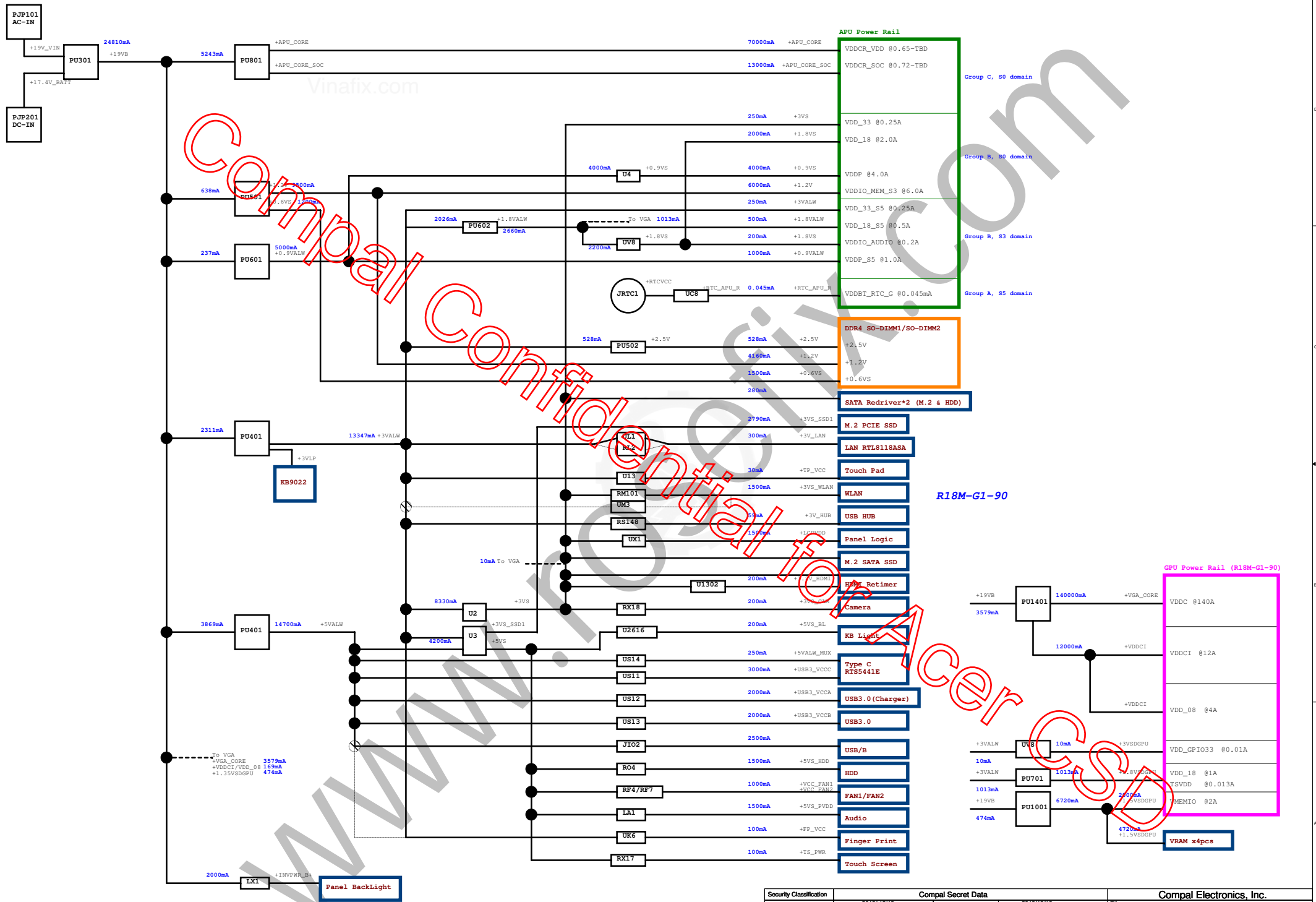
POWER SEQUENCE

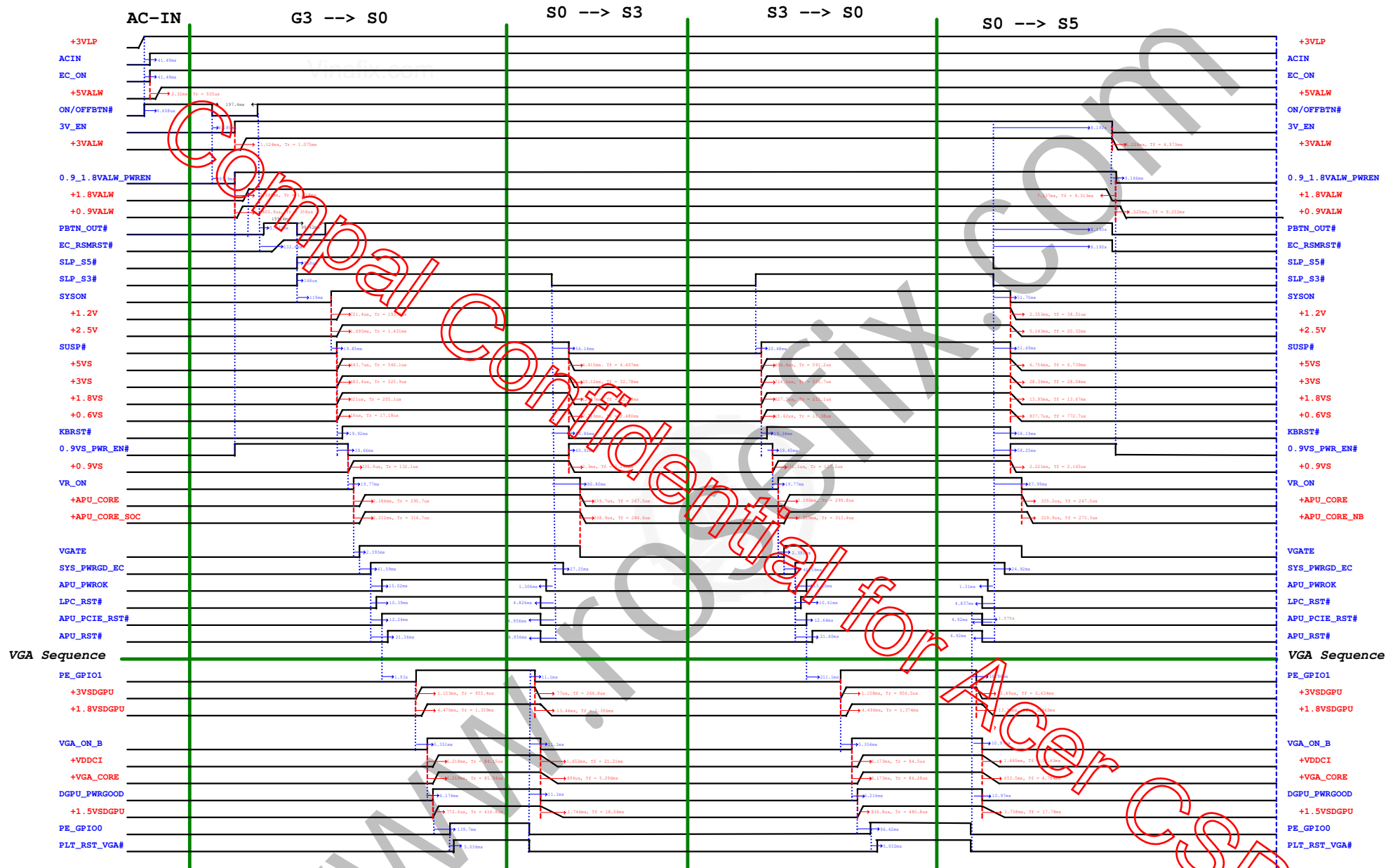


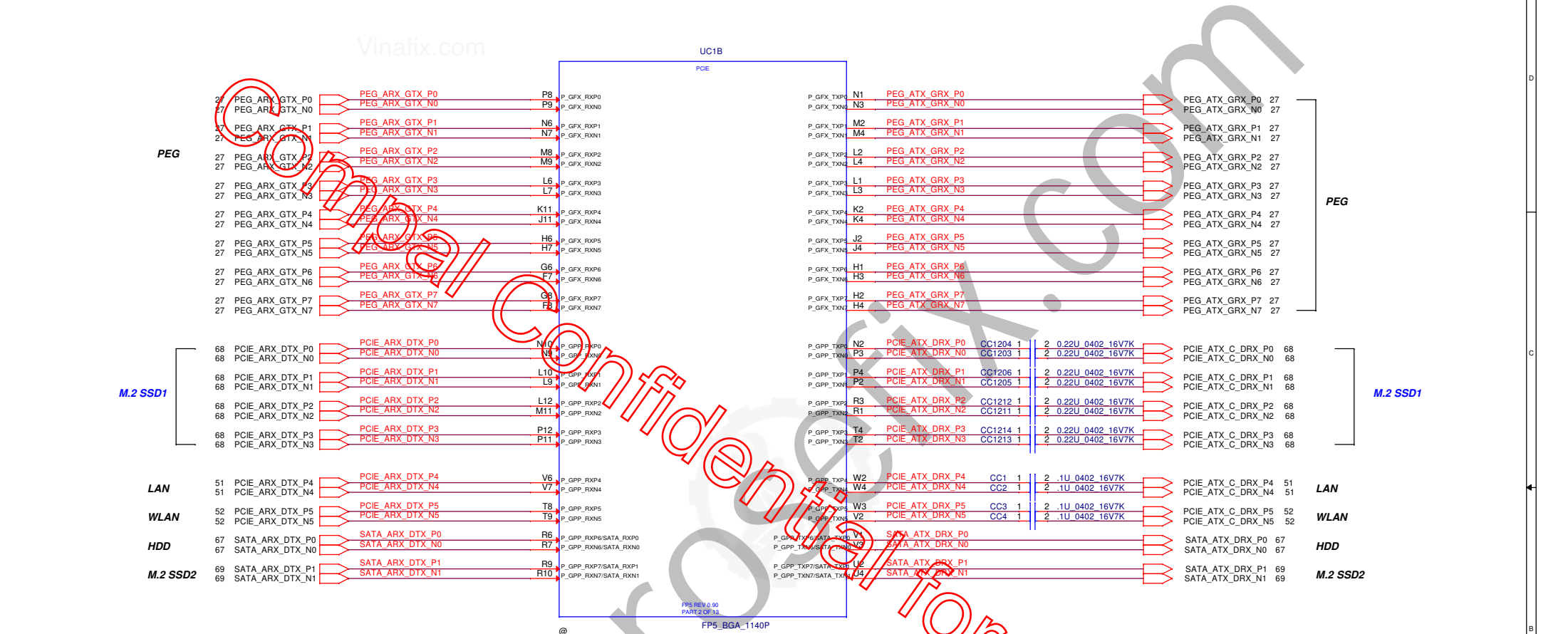
VGA POWER SEQUENCE



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APU PN Table

APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN	Compal PN
Picasso	UC1 R5APUQC@ S IC RYZEN5 YM3500C4T4MFG 2.1G BGA APU SA0000CCR20	UC1 R7APUQC@ S IC RYZEN7 YM3700C4T4MFG 2.3G BGA APU SA0000C7640	UC1 R5APU@ S IC RYZEN5 YM3500C4T4MFG 2.1G APU ABO! SA0000CCR60	UC1 R7APU@ S IC RYZEN7 YM3700C4T4MFG 2.3G APU ABO! SA0000C7680		

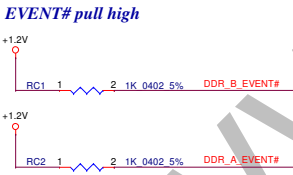
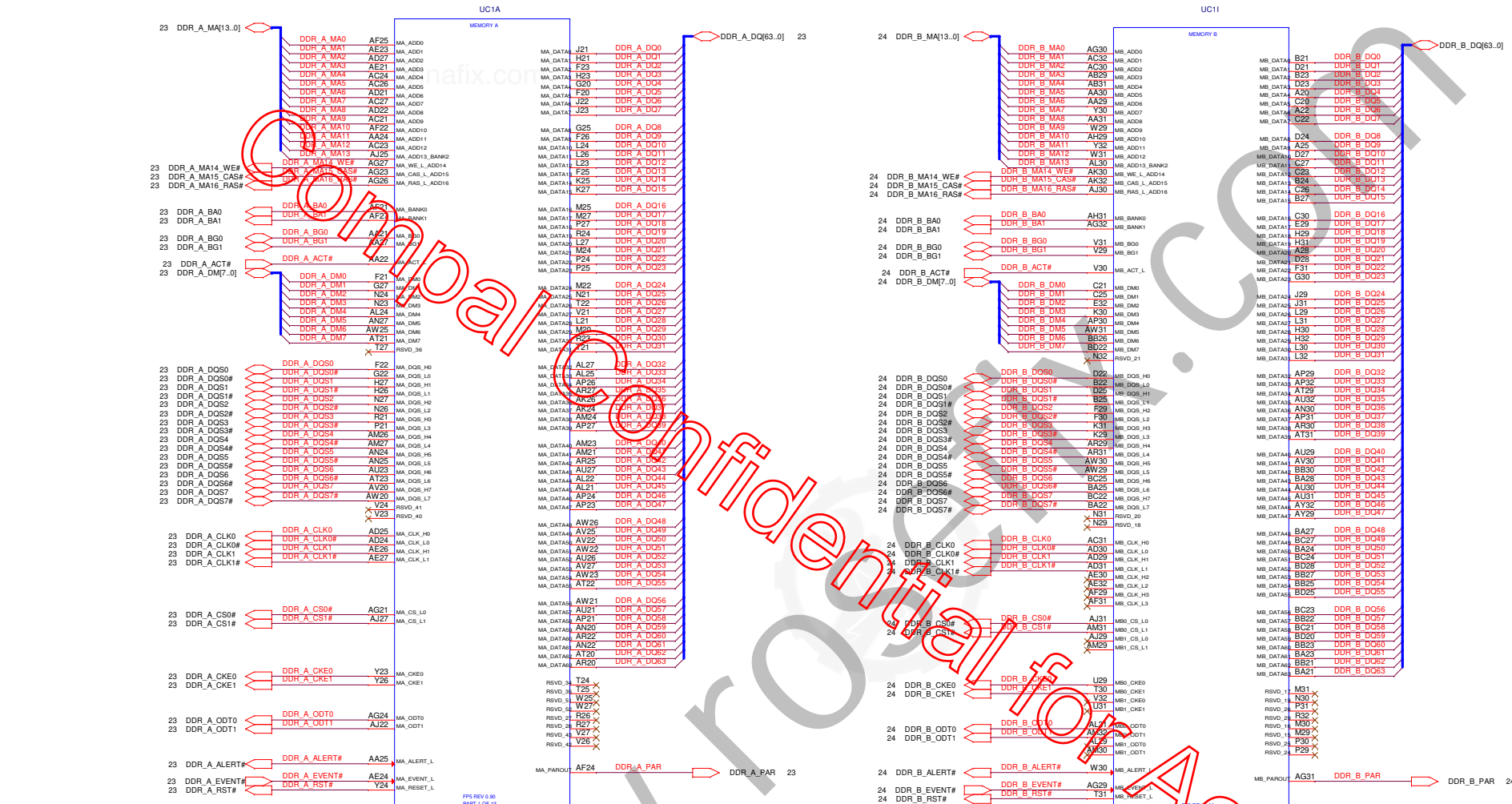
PCB Number

ZZZ EVT@
PCB 2QE LA-H901P REV0 MB 2
DA8001JM000

ZZZ PVT@
PCB FH50P LA-H901P LS-H901P/H502P
DAZ2QE00100
PCB: DAZ2QE00100, DA8001JM010 REV: 1.0/1.0/1.0

ZZZ MP@
PCB FH50P LA-H901P LS-H901P/H502P
DAZ2QE00101
PCB: DAZ2QE00101, DA8001JM01A REV: 1.A/1.0/1.0

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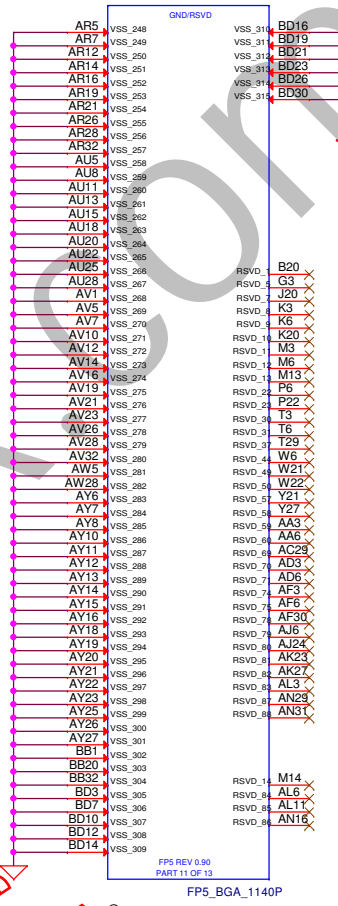
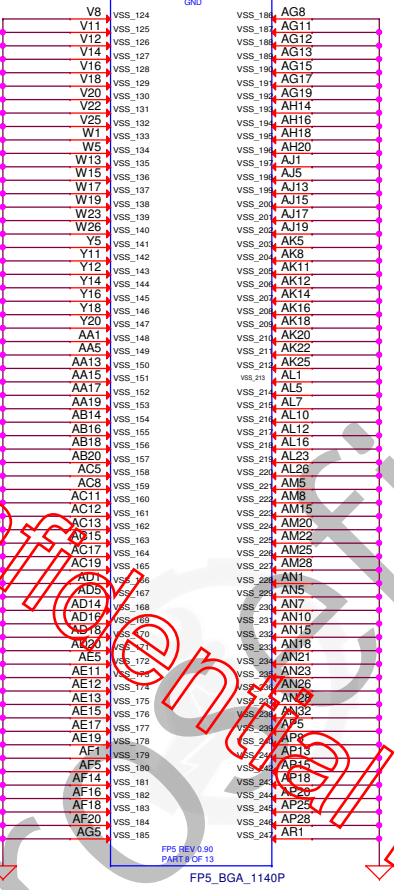
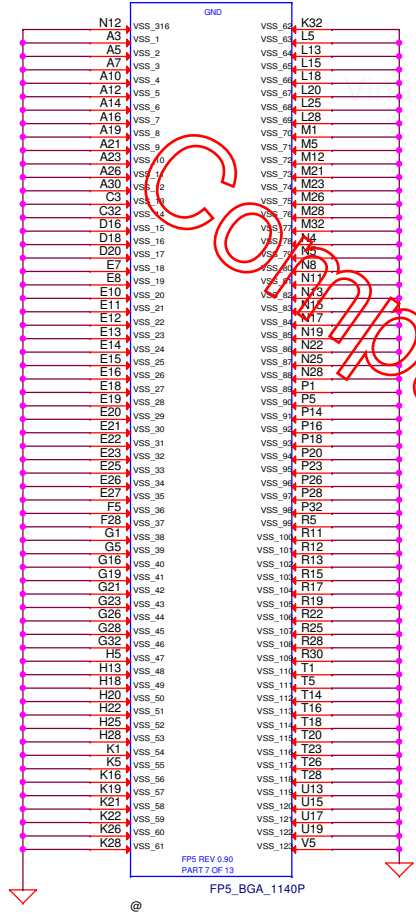


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UC1G

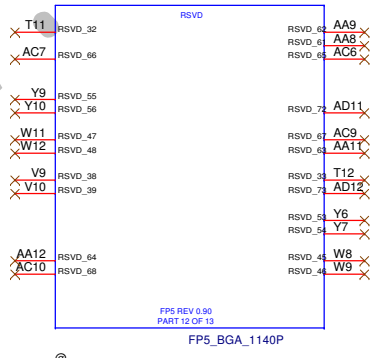
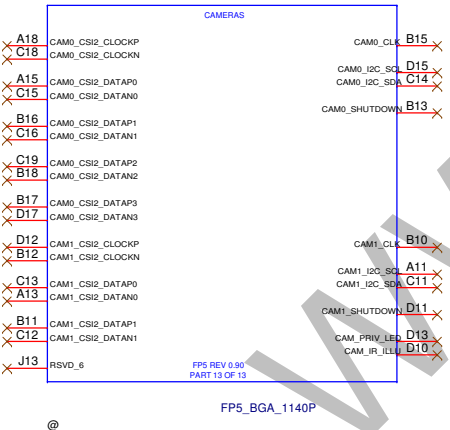
UC1H

UC1K



UC1M

UC1L



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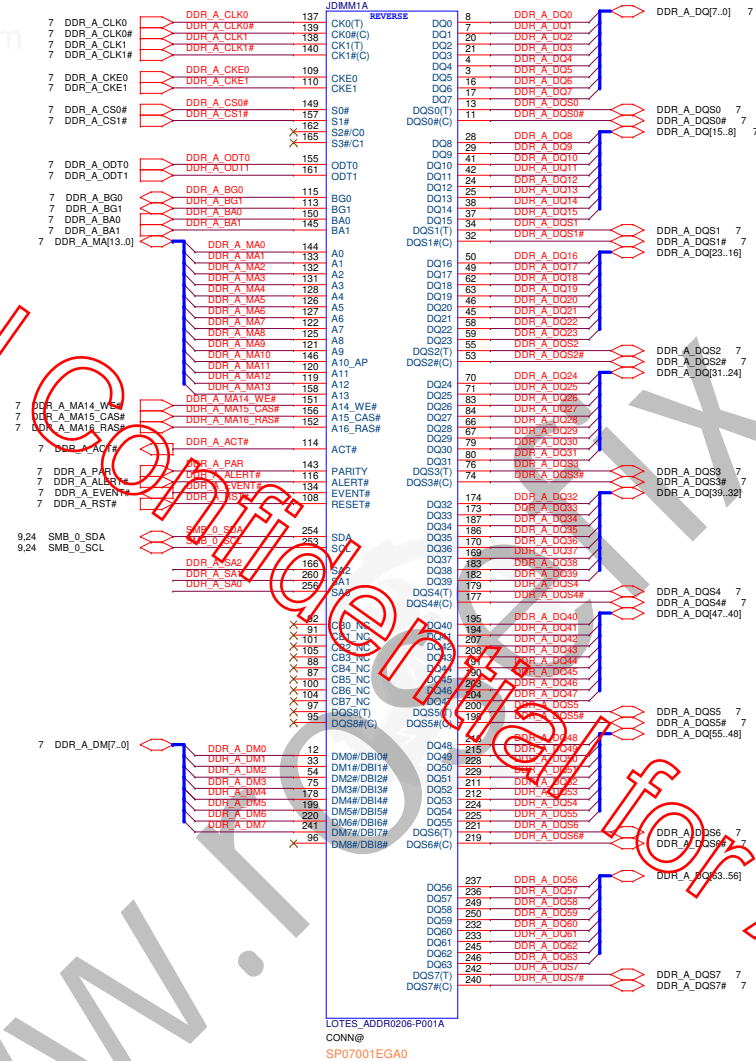
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

CRB use 0.1uF x12 (6 pop, 6 unpop), 180pF x1, 100uF x2

Follow MA51

© CD18
330U_D2_2V_V

SGA00008S00
330U 2V H1.9
9mohm POLY



Pinout diagram for the LOTES_ADDR0206-P001A connector. The diagram shows two rows of pins. The top row has pins 111 to 156, with labels for JDM1B, VDD1 to VDD10, VDDSPD, VREFCA, and VPP1 to VPP2. The bottom row has pins 1 to 100, with labels for VSS, VDD1 to VDD19, VSS, VDD20 to VDD25, and VSS. Power connections are shown: +1.2V to pins 111, 112, 117, 118, 123, 124, 129, 130, 135, 136; +3V5 to pins 111, 112, 117, 118, 123, 124, 129, 130, 135, 136; +1.2V to pins 141, 142, 147, 148, 153, 154, 159, 160, 163; +0.6V5 to pins 141, 142, 147, 148, 153, 154, 159, 160, 163; and +2.5V to pins 255, 257, 259, 261. A capacitor CD33 (1uF, 0.01V) is connected between pins 257 and 259. The diagram is labeled 'f.' on the left and 'SP07001G0A0' at the bottom.

CRB use 4.7uF x1, 0.1uF x1

+0.6V5

CD30

100nF 0.0001 3.3V6M

100nF 0.0001 3.3V6M

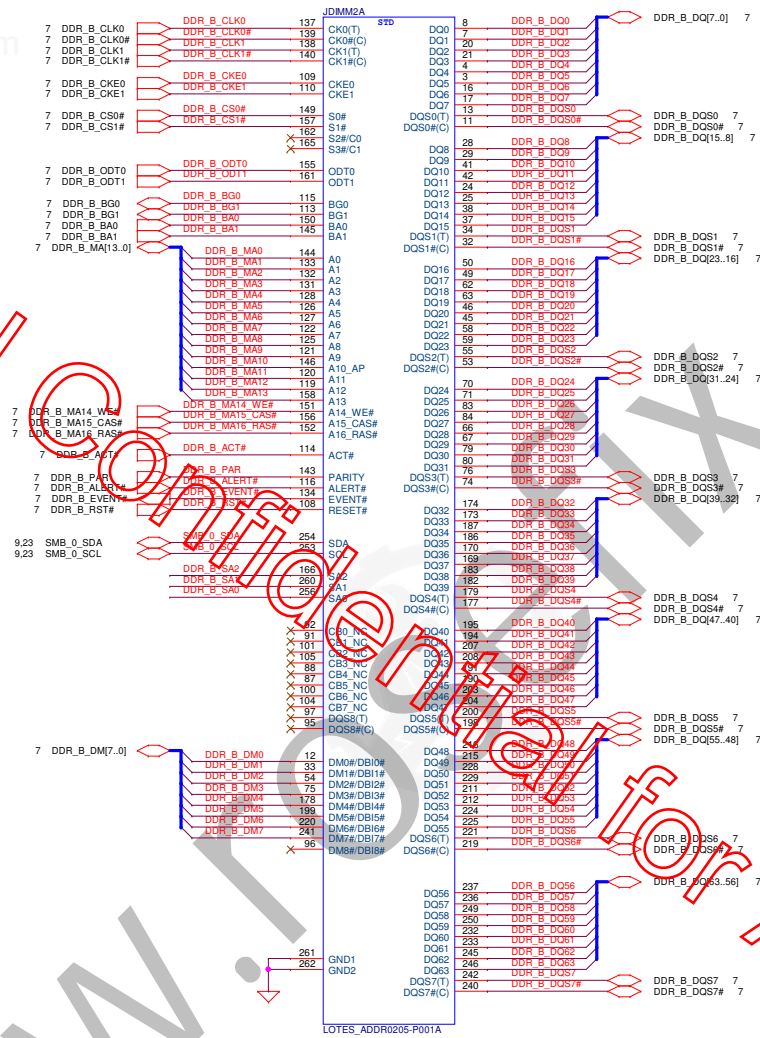
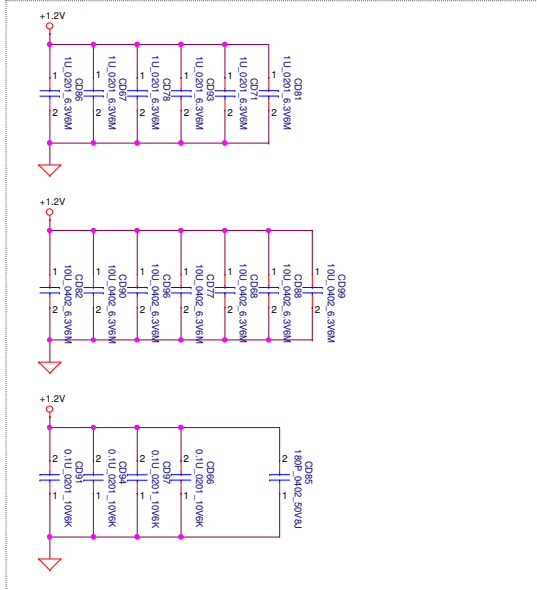
0.1uF 0.0001 3.3V6M

3.3V

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Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

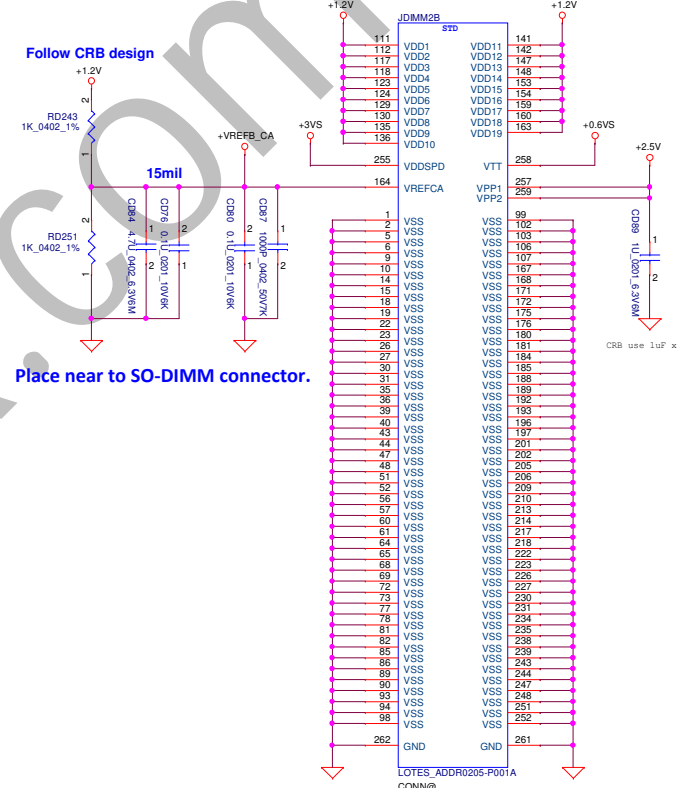
CRB use 0.1uF x12 (6 pop, 6 unpop), 180pF x1, 100uF x2



Follow CRB design

15mil

Place near to SO-DIMM connector.



The circuit diagram shows an operational amplifier (CD70Z) configured as a voltage follower or buffer. The non-inverting input (+) is connected to the +0.6V source. The inverting input (-) is connected to the output through a feedback resistor labeled CRD (100k). There is also a feedback path from the output to the inverting input through a resistor labeled CRB (10k). The output is connected to a load resistor RL (100k) which is grounded. A red circle highlights the feedback loop consisting of CRB and CRD.

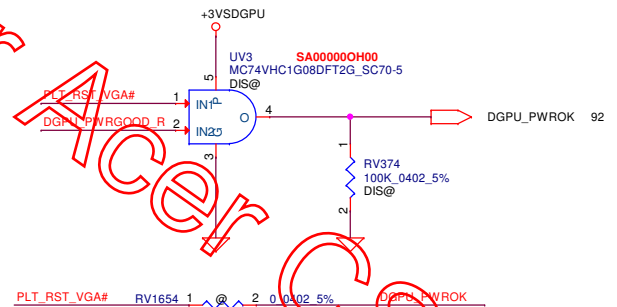
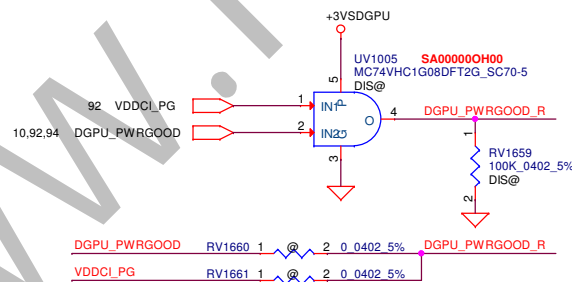
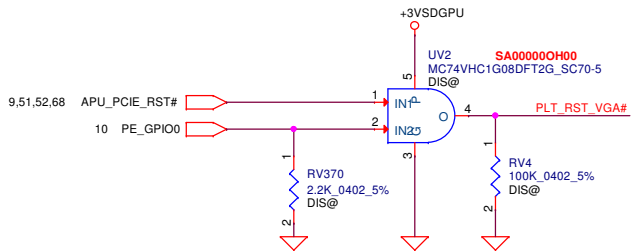
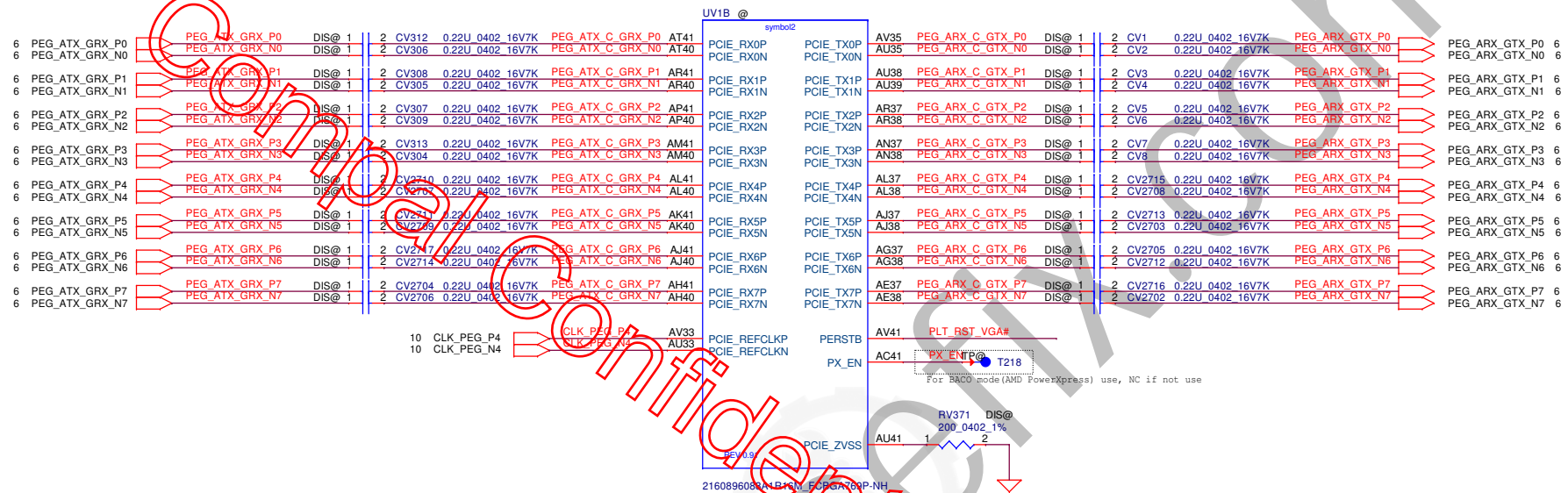
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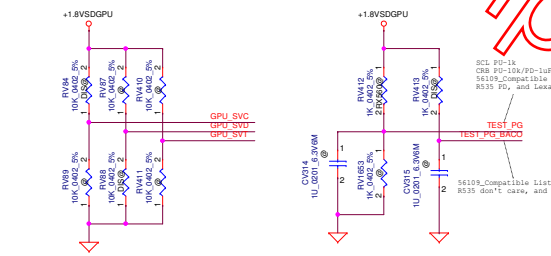
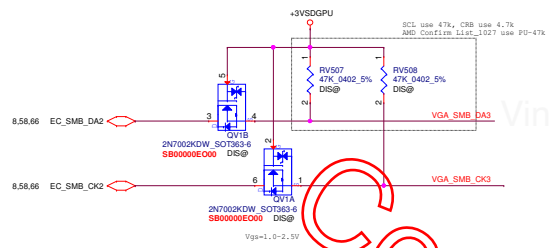
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Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

RX560 Strap

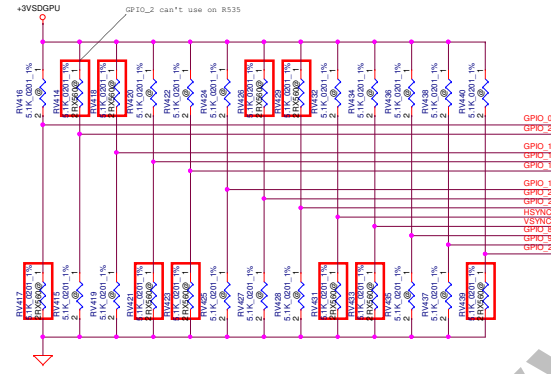
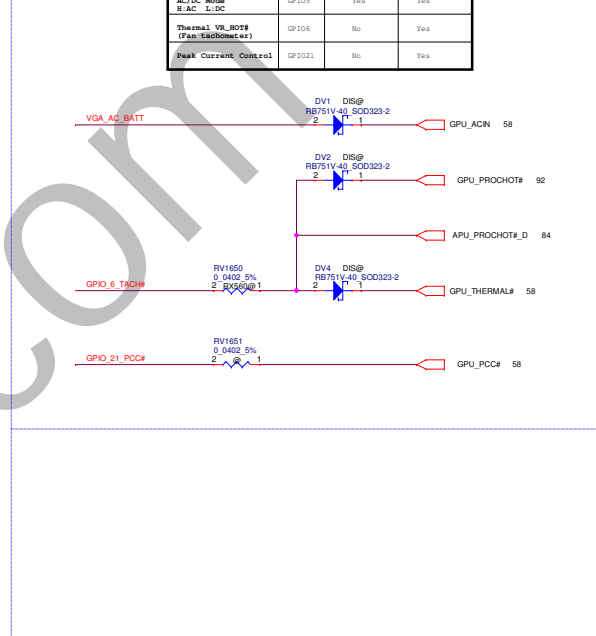
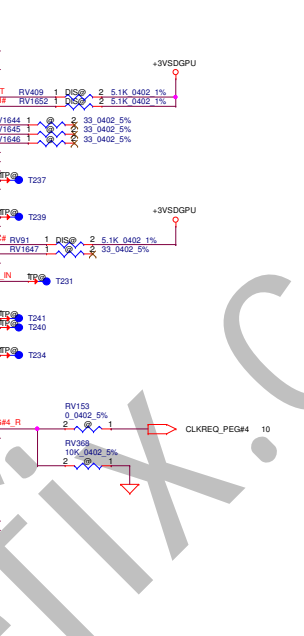
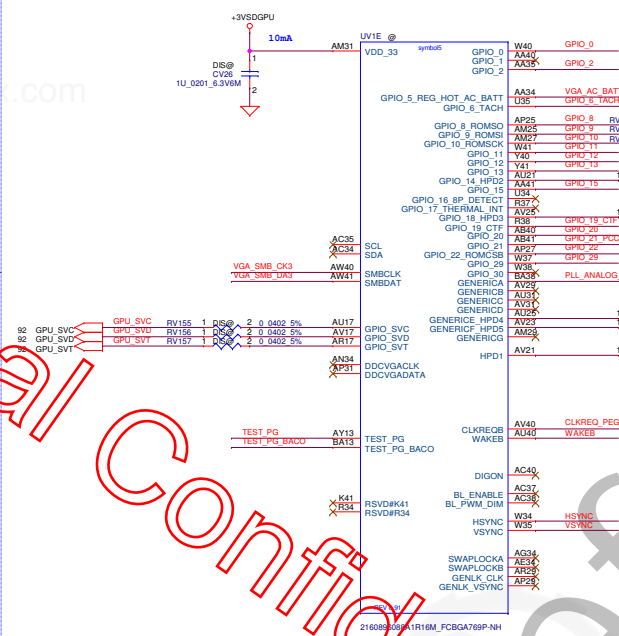


Table 3-27 Primary Memory Aperture Sizes Requested at PCI Configuration

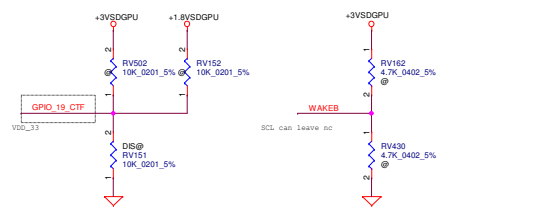
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

3.2.2.2 ROM Configurations

- For designs that have a dedicated ROM device for the GPU video BIOS:
- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
 - Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

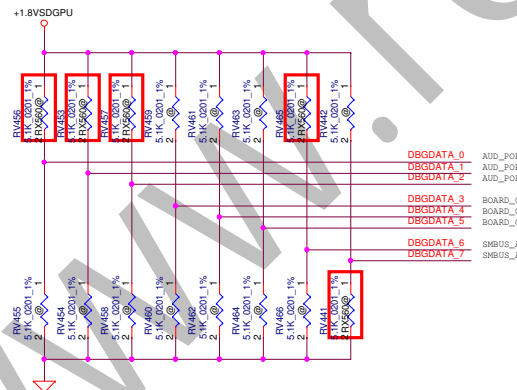
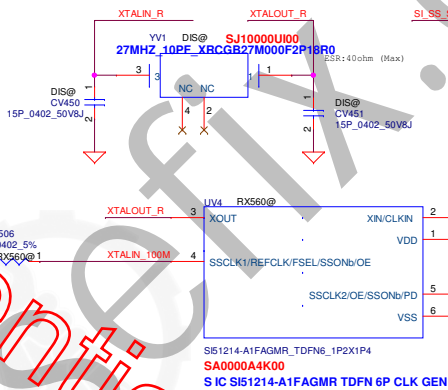
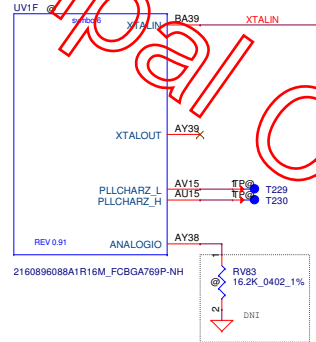
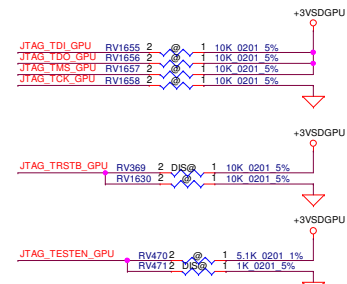
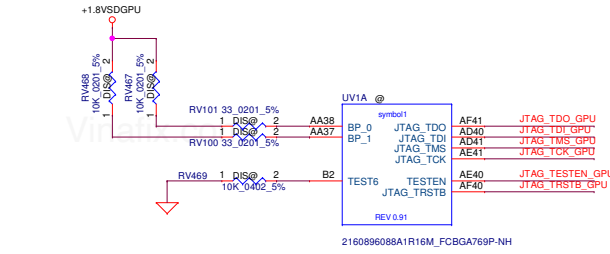


Function Support	Pin	R18M-G1-90	R18M-G1-90/75
AC/DC Mode	GP105	Yes	Yes
Thermal_VR_HOT# (Fan tachometer)	GP106	No	Yes
Peak Current Control	GP1021	No	Yes



UV1K @	symbol11	
DBGDATA_0	L40	DBGDATA_0
DBGDATA_1	L41	DBGDATA_1
DBGDATA_2	M40	DBGDATA_2
DBGDATA_3	M41	DBGDATA_3
DBGDATA_4	N40	DBGDATA_4
DBGDATA_5	N41	DBGDATA_5
DBGDATA_6	P40	DBGDATA_6
DBGDATA_7	P41	DBGDATA_7
DBGDATA_8	R40	DBGDATA_8
DBGDATA_9	R41	DBGDATA_9
DBGDATA_10	T40	DBGDATA_10
DBGDATA_11	T41	DBGDATA_11
DBGDATA_12	U40	DBGDATA_12
DBGDATA_13	U41	DBGDATA_13
DBGDATA_14	V40	DBGDATA_14
DBGDATA_15	V41	DBGDATA_15

REV:0.91
2160896088A1R16M_FCBGA769P-NH



AUD_PORT_CONN [2:0]
* 111: No usable endpoints
110: One usable endpoint
101: Two usable endpoints
100: Three usable endpoints
011: Four usable endpoints
010: Five usable endpoints
001: Six usable endpoints
000: All endpoints are usable

BOARD_CONFIG [2:0]
000: SMI 256Mx32 (8Gb)
001: Hynix 256Mx32 (8Gb)
010:
011:
100:
101:
110:
111:

DBGDATA [7:6]
* 00: 0x40
* 01: 0x41
* 10: 0x42
* 11: 0x43

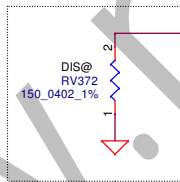
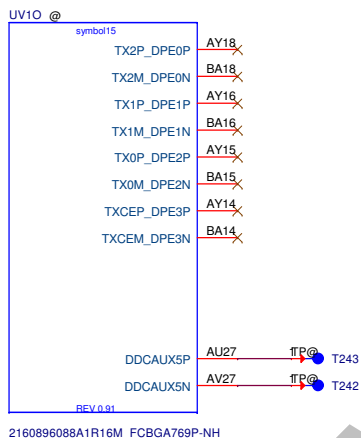
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				Size		Document Number		Rev	
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				Date				Wednesday, May 15, 2019	



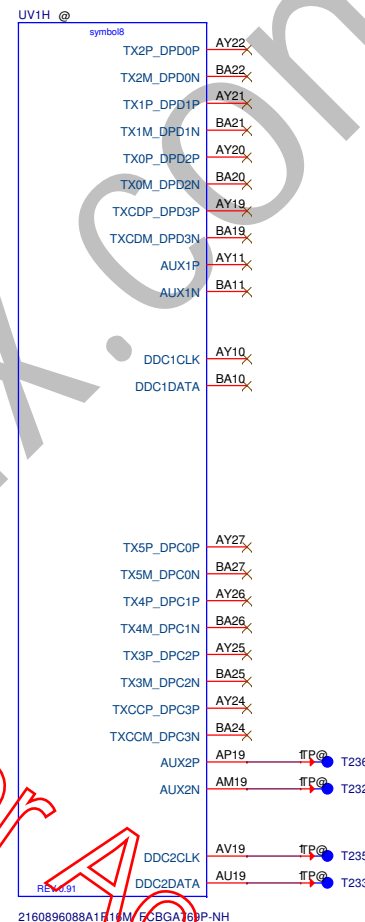
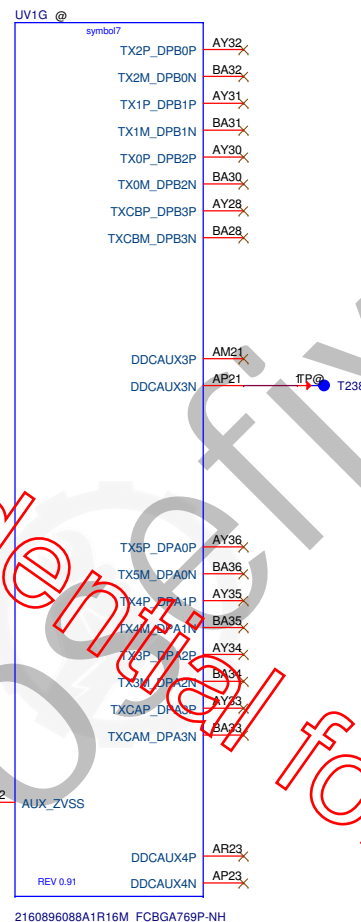
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Vinafix.com

Compal Confidential for Acer CSD



Data Book: need config even if not use display function



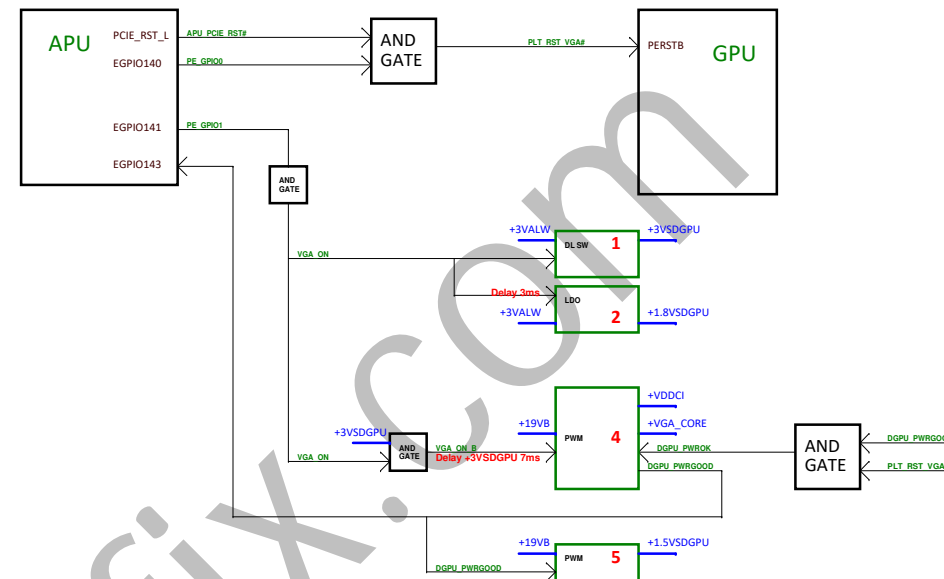
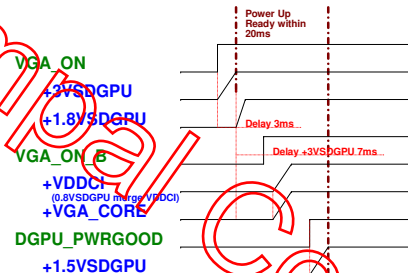
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5.3 Power-up/down Sequence

"R17M-G1-50 / R17M-G1-70 / R18M-G1-90" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/ μ s.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μ s before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

R18M-G1-90



For AMD R18M-G1-90 VRAM Device ID: 67EF/C0

Memory ID/Vendor/Size	Memory PN R3(ABOI)	BOARD_CONFIG[2:0]
000 (8Gb) SAMSUNG 256M x32	UV1001 X78_S4G@ UV1002 X78_S4G@ UV1003 X78_S4G@ UV1004 X78_S4G@ S IC D5 256M32 K4G0325FB-HC25 FBGA ABO! SA00009TA10	RV464 X78_S4G@ RV462 X78_S4G@ RV460 X78_S4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900
001 (8Gb) HYNIX 256M x32	UV1001 X78_H4G@ UV1002 X78_H4G@ UV1003 X78_H4G@ UV1004 X78_H4G@ S IC D5 256M32 H5GC8H24AJR-R2C BGA ABO! SA0000C1700	RV464 X78_H4G@ RV462 X78_H4G@ RV460 X78_H4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900
010 SAMSUNG 128M x32		
011 HYNIX 128M x32		
100 MICRON 256M x32		

AMD GPU PN

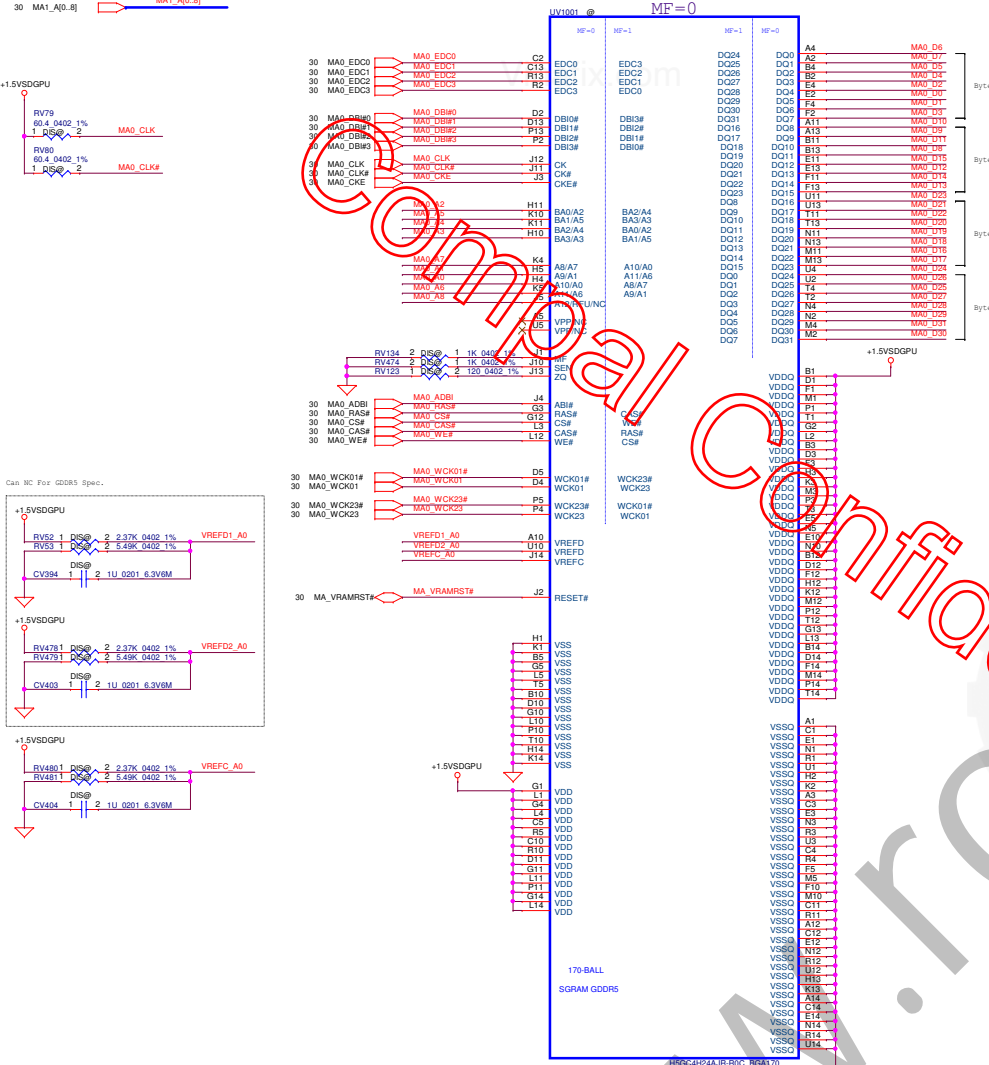
R18M-G1-90 PN R1(ROH)
UV1 RX560@
S IC 215-0908004 A1 R18M-G1-90 ABO! SA0000BFF10

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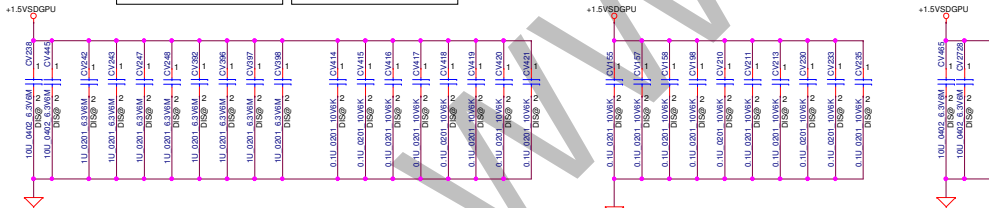


A0 Channel

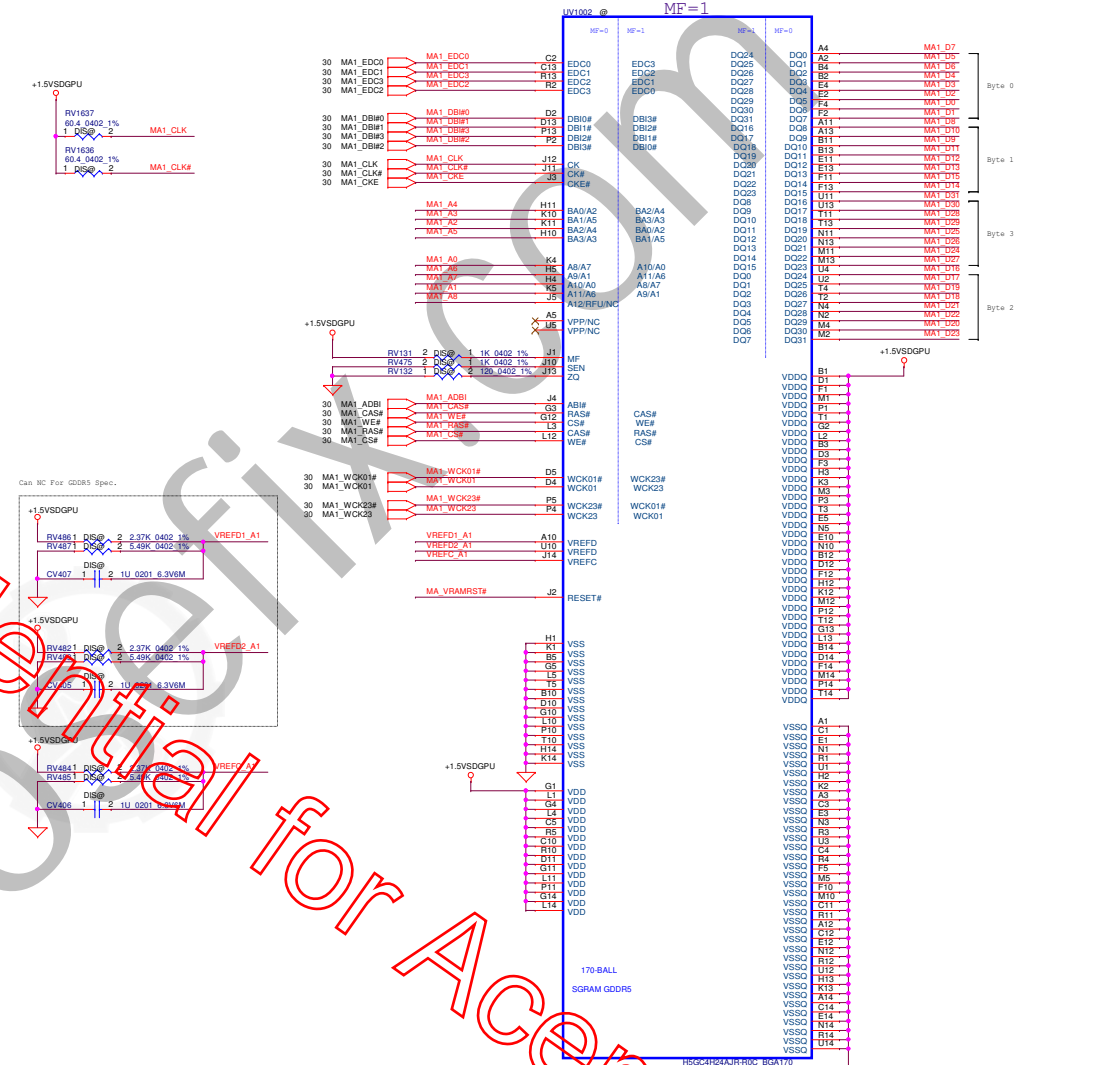


Decoupling Caps for single-sided
1x 100pF / per DRAM
8x 10uF / per DRAM
8x 0.1uF / per DRAM

Decoupling Caps for C144
1x 100pF / per DRAM
8x 10uF / per DRAM
8x 0.1uF / per DRAM



A1 Channel

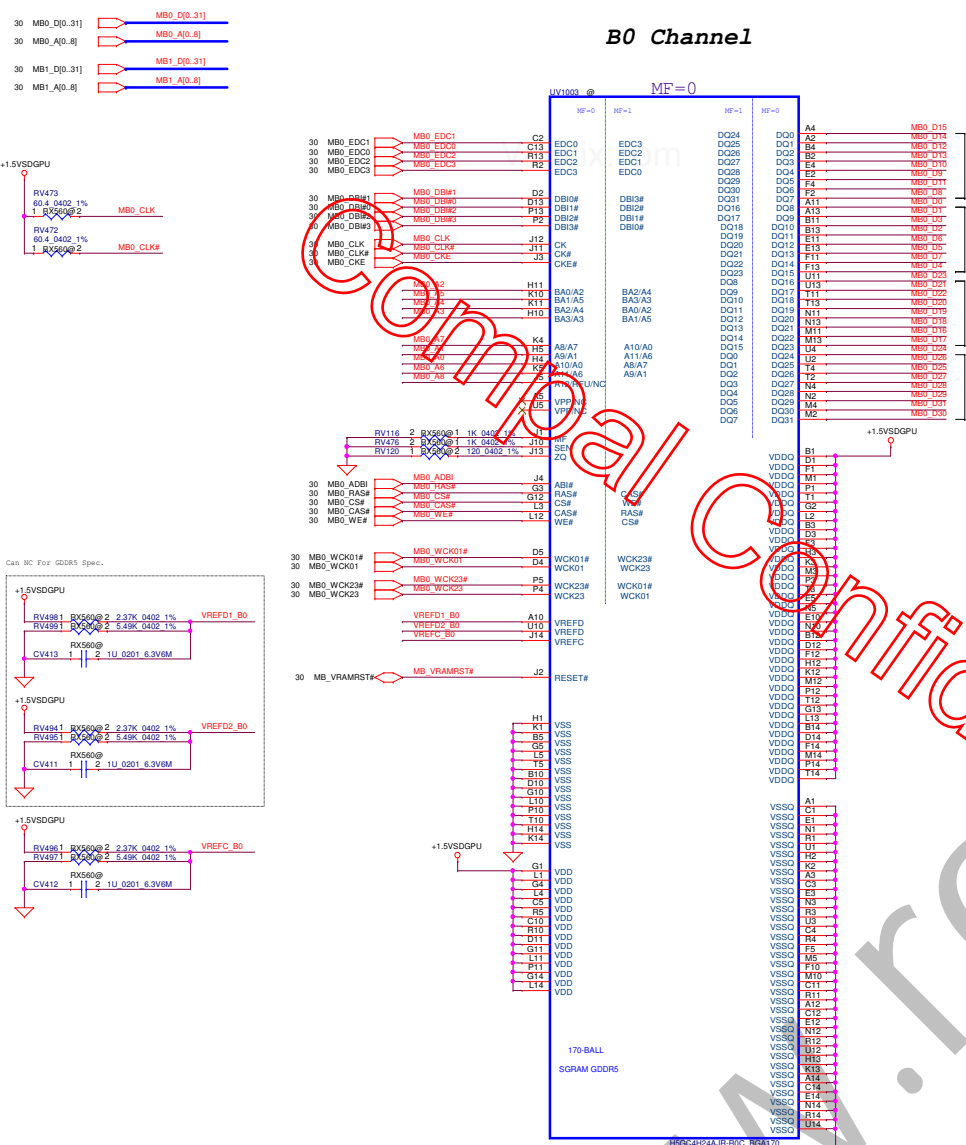


Decoupling Caps for single-sided
1x 100pF / per DRAM
8x 10uF / per DRAM
8x 0.1uF / per DRAM

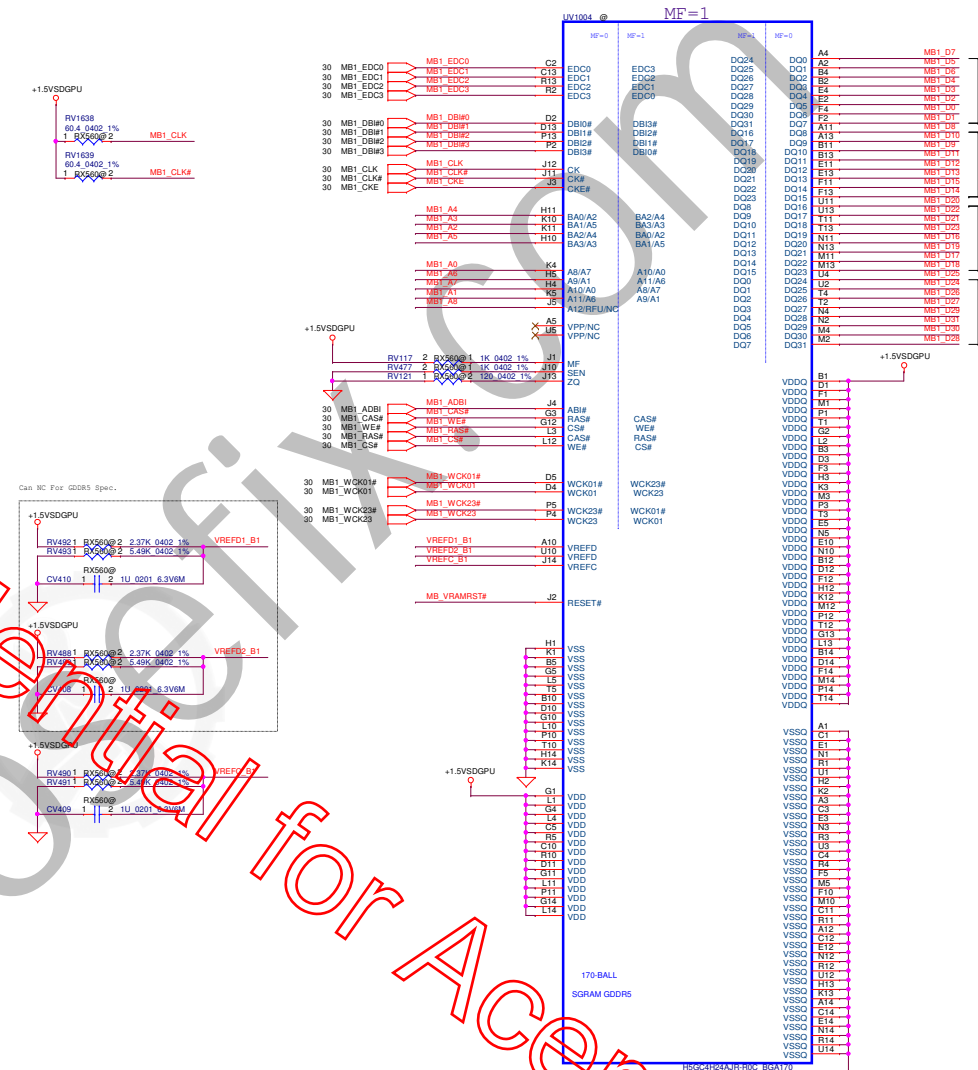
Decoupling Caps for C144
1x 100pF / per DRAM
8x 10uF / per DRAM
8x 0.1uF / per DRAM



B0 Channel



B1 Channel

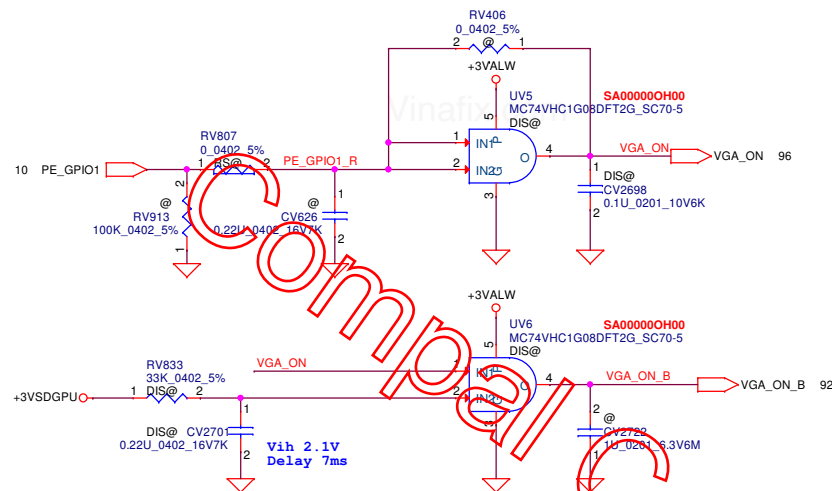


Decoupling Caps for single-sided 1x 10uF /per DRAM 8x 1uF /per DRAM 8x 0.1uF /per DRAM	Decoupling Caps for Clanshell 1x 10uF /per Clanshell DRAM 8x 1uF /per Clanshell DRAM
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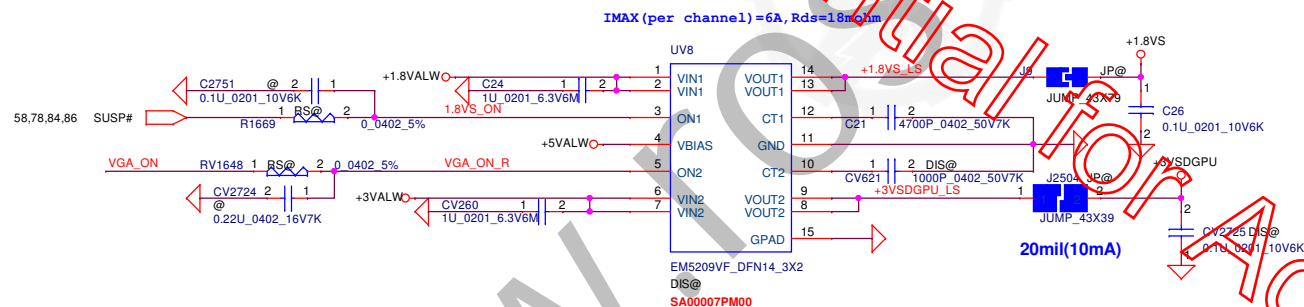
Box Layout: Nocebo Effect

Box Layout: Antenna Effect

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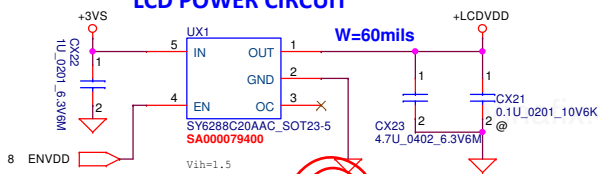


+3VALW TO +3VSDGPU

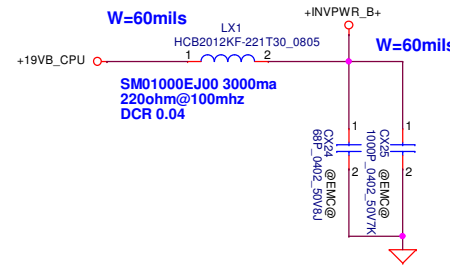
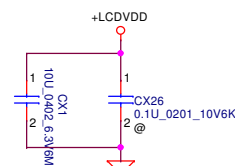


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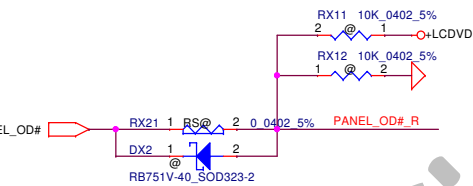
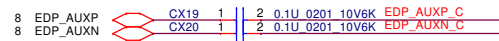
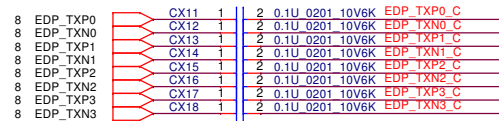
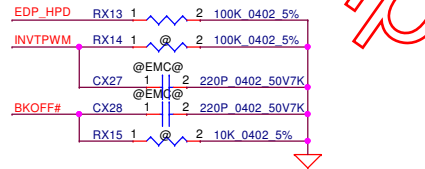
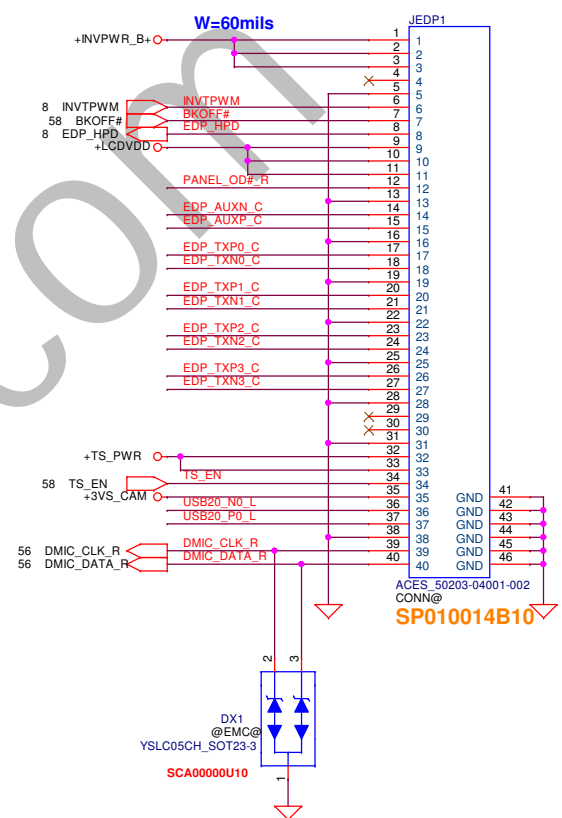
LCD POWER CIRCUIT



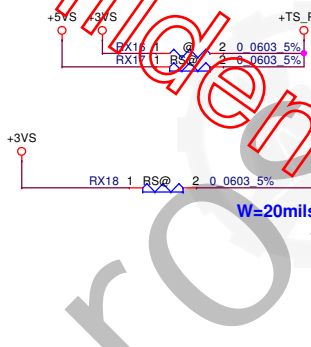
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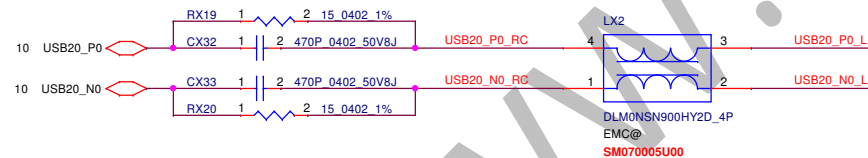
LED PANEL Conn.



Touch Screen



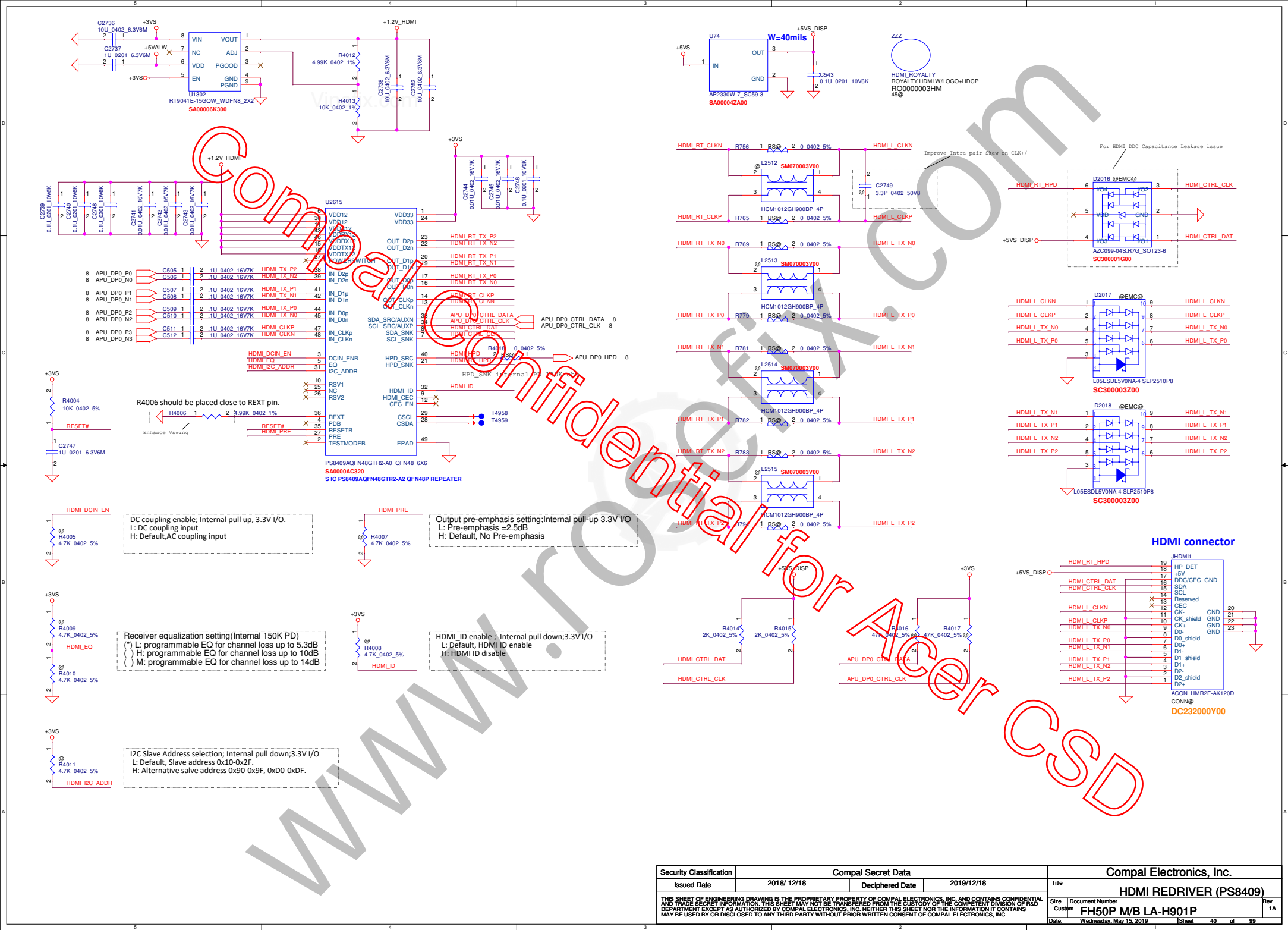
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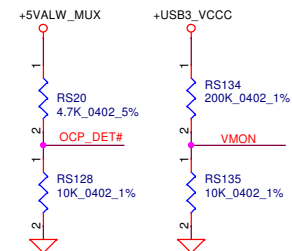
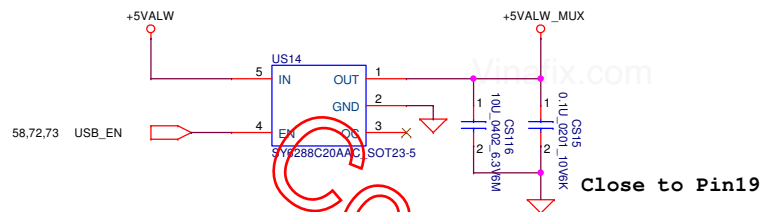
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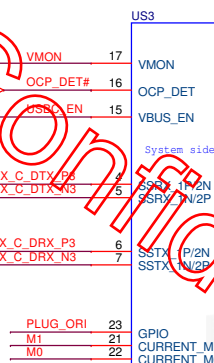
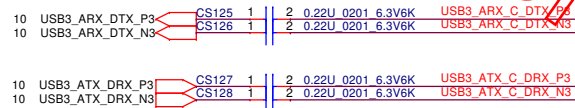
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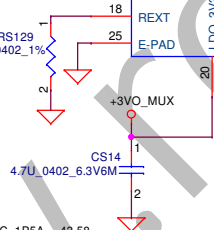
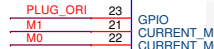
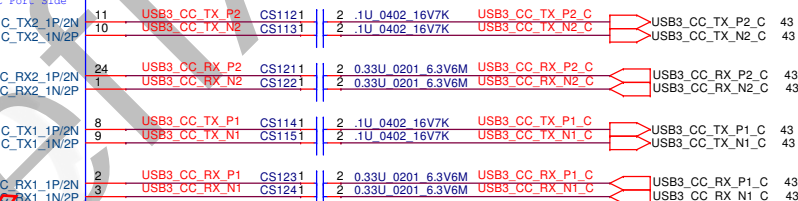
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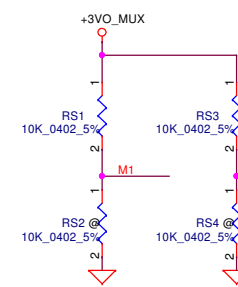
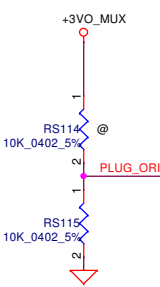
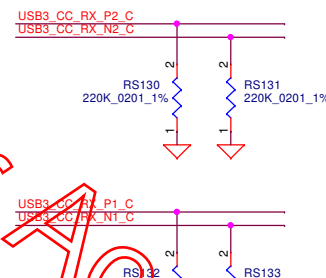
USB3.0 (Port 3)



Type-C Port Side



Close to Pin13

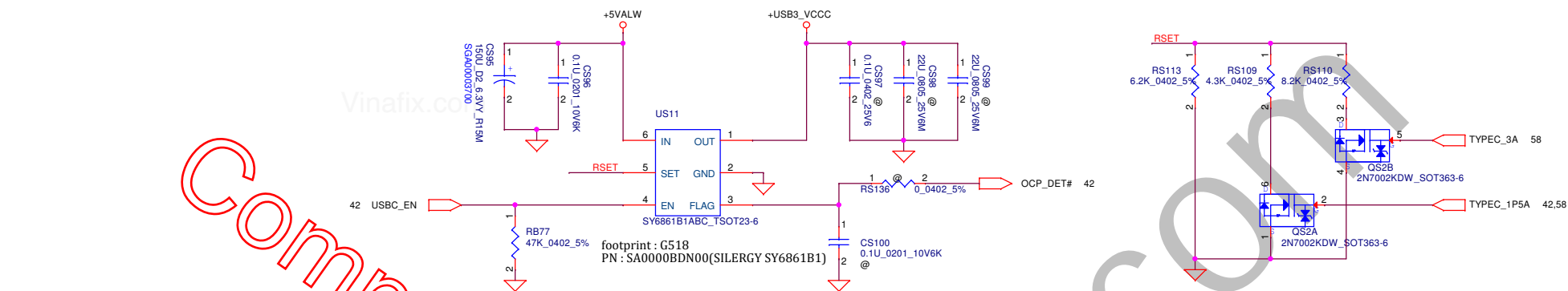


RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

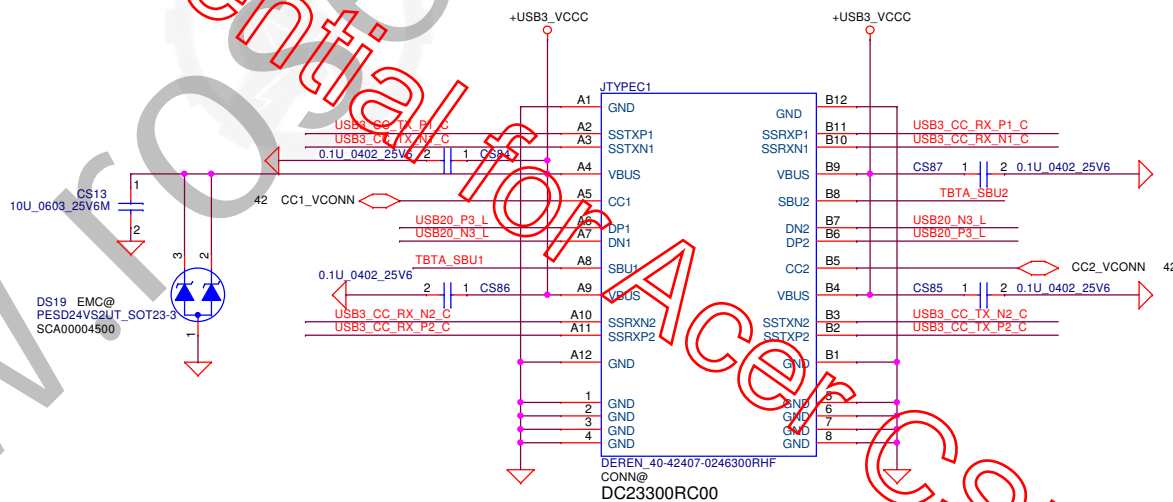
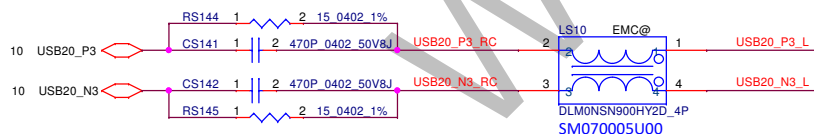
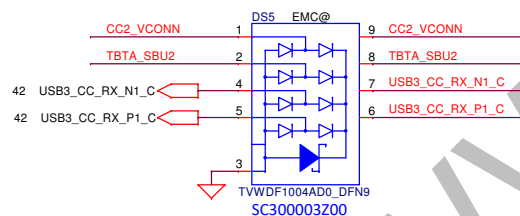
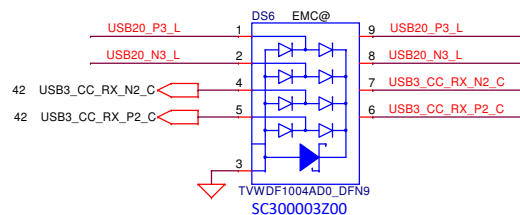
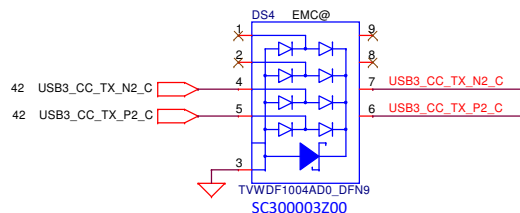
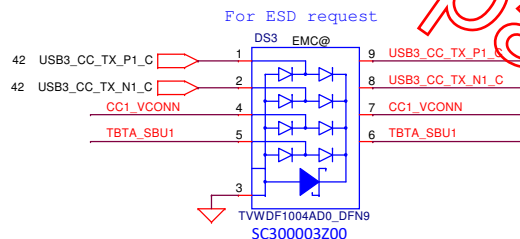
5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

confirm realtek hand-shake

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SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20mil trace width.

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				Size	Document Number	Rev
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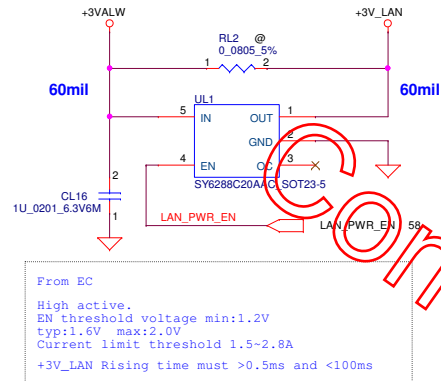
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				Rev	1A

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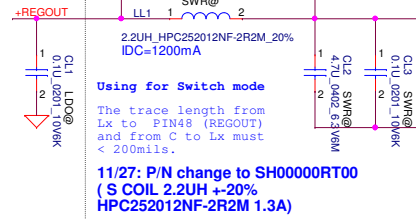
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+3V_LAN Rising time (10%-90%) must >0.5mS and <100mS

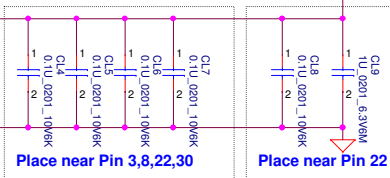


RTL8111H LDO mode
RTL8118ASA SWR mode

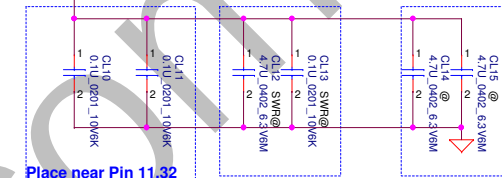
W=60mil



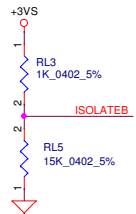
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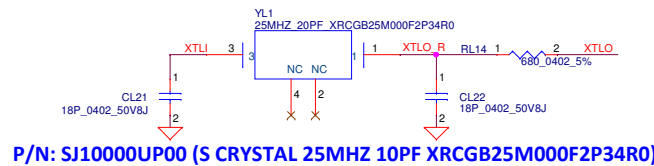
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300mA



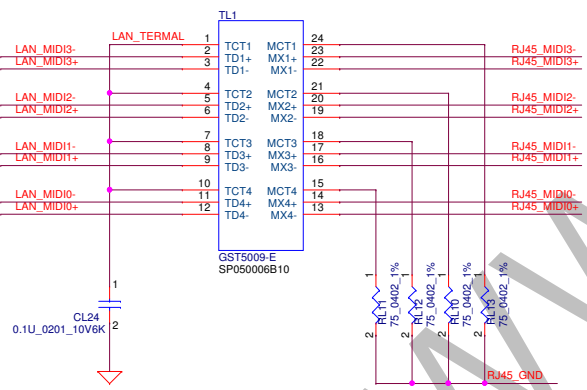
Reserve for surge improvement
Place near Pin 11,32



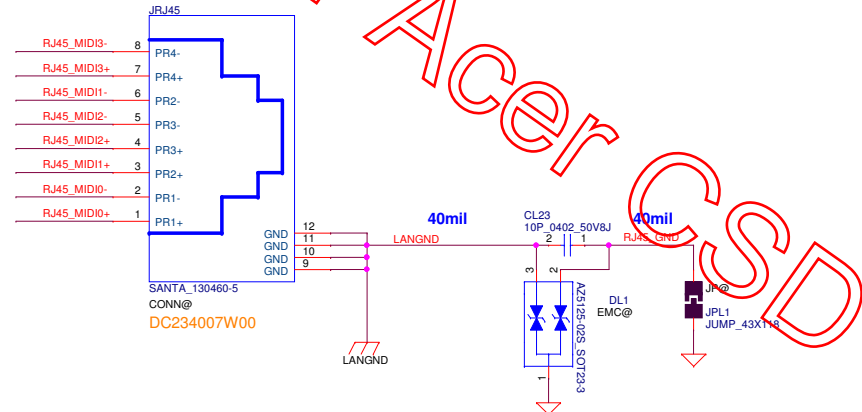
LAN_CLKREQ# pull up at PCH side



SA0000B9F20, S IC RTL8118ASA CG QFN 32P E-LAN CTRL

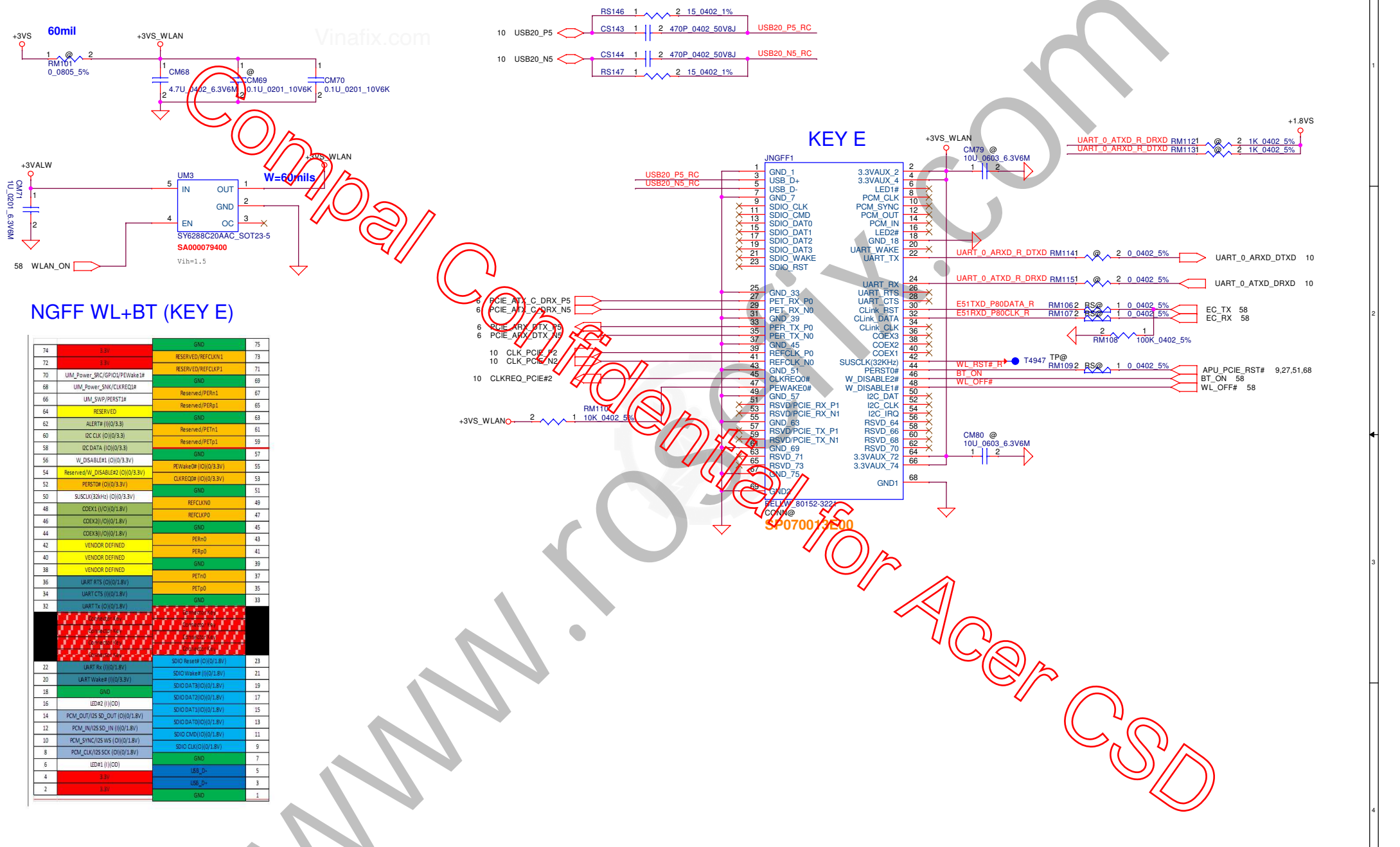


LAN Connector



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Wireless LAN



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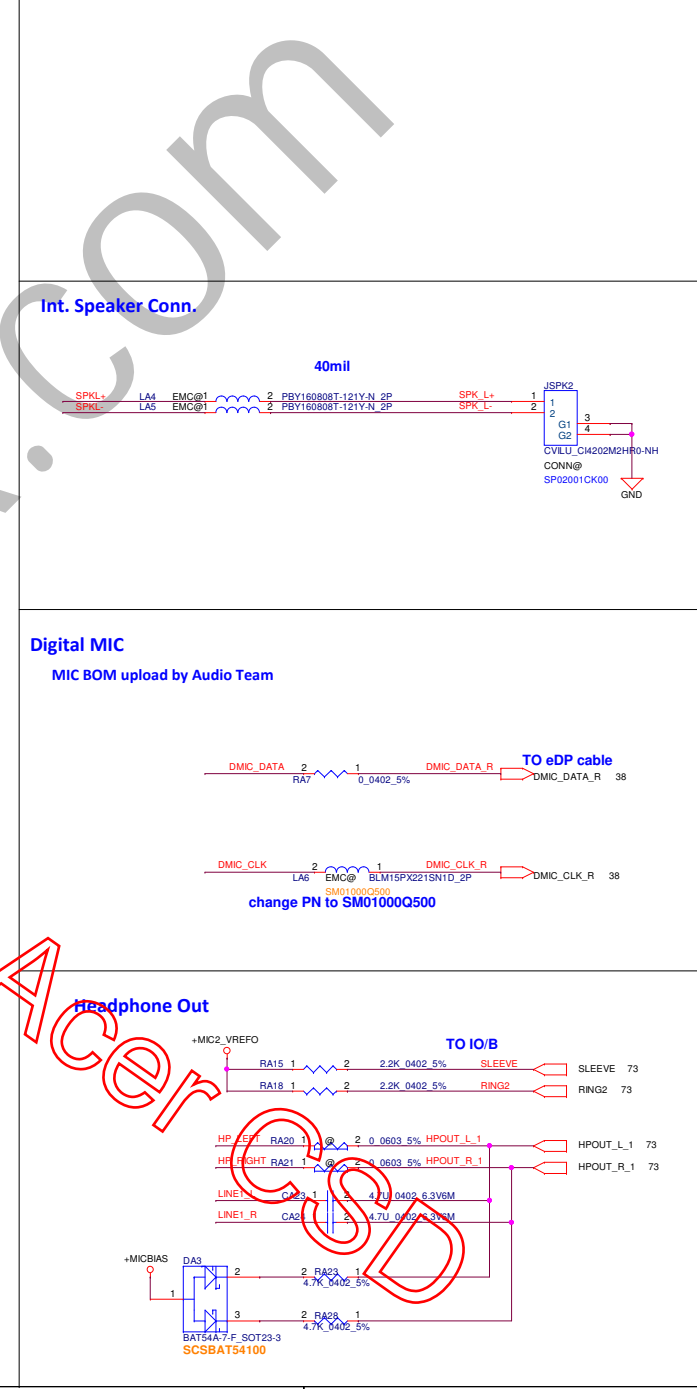
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				Size	Document Number	Rev
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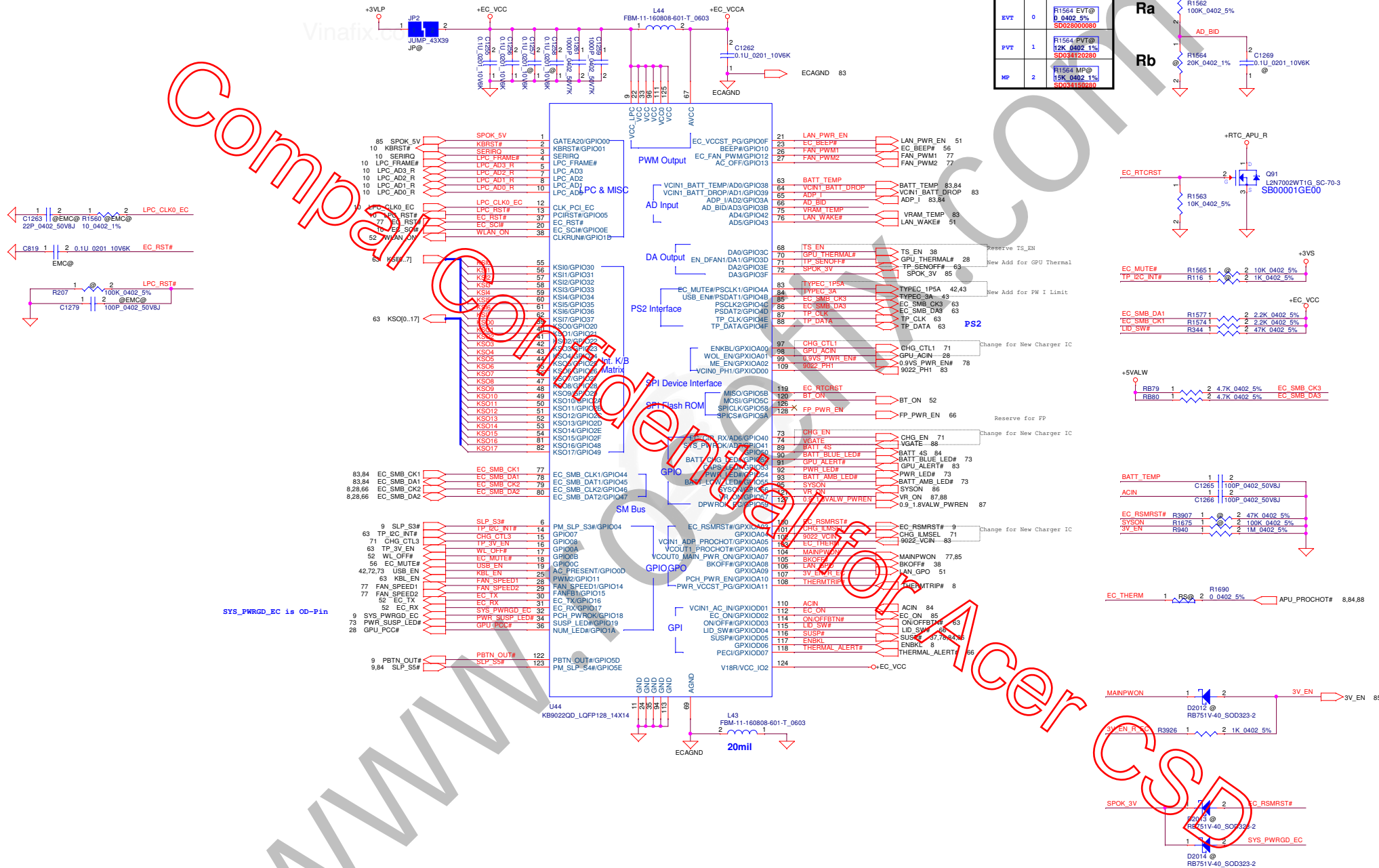
2000mA 600ohm@100MHz
DCR 0.1



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Board ID / Rb			
SVT	0	R1564 EVT@	B 0402 5% SD028000080
PVT	1	R1564 PVT@	D 0402 1% SD034120280
MP	2	R1564 MP@	L 9K 0402 1% SD034120280

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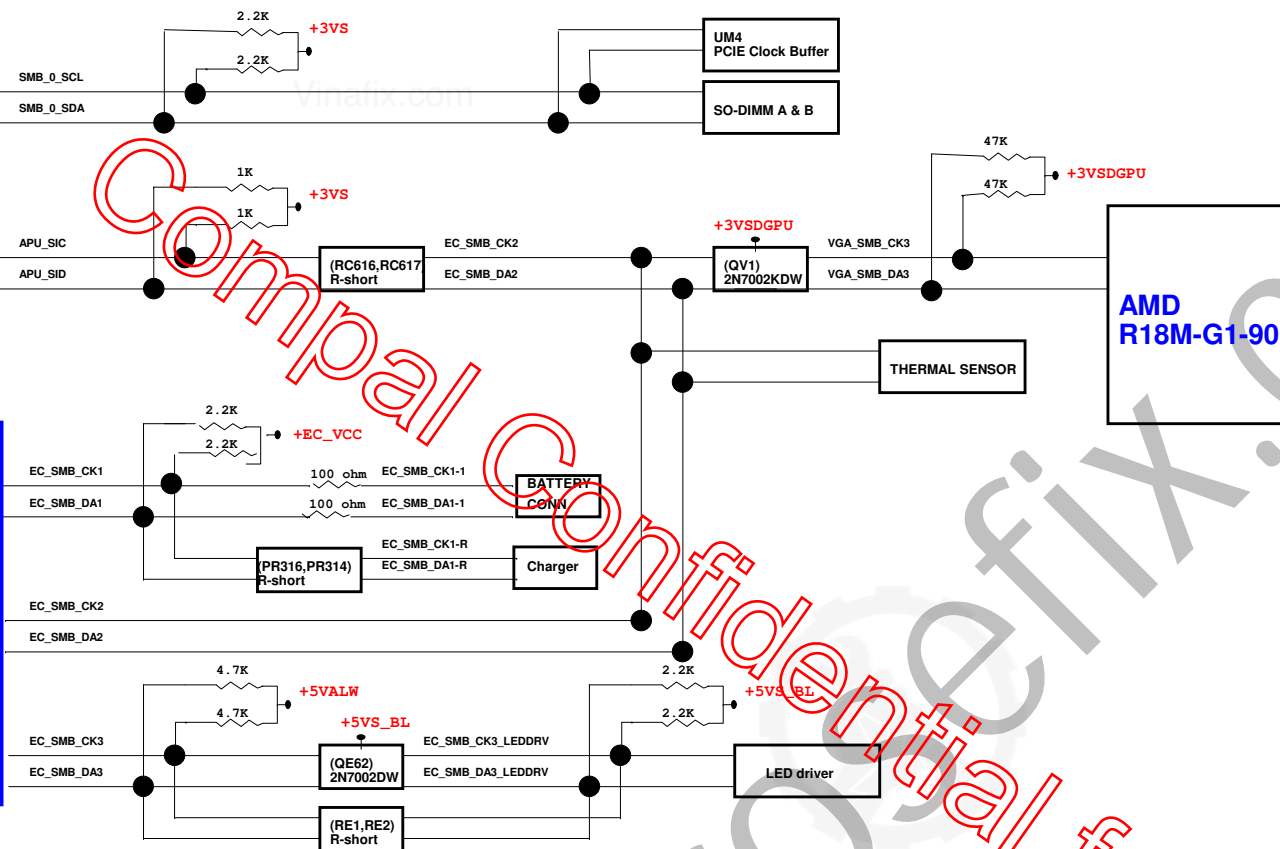
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13C3_SCL/EEP10113/SCLO
13C3_SDA/EEP10114/SDAO

**Picasso
APU**

KB9022

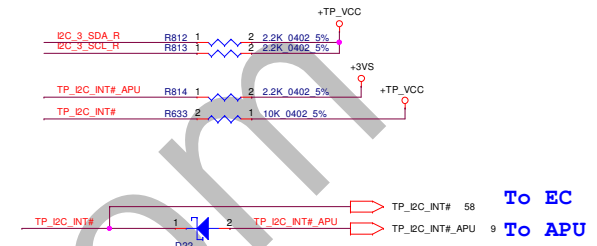
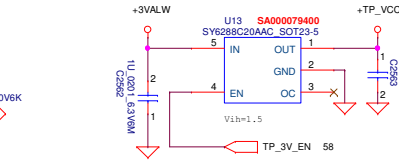
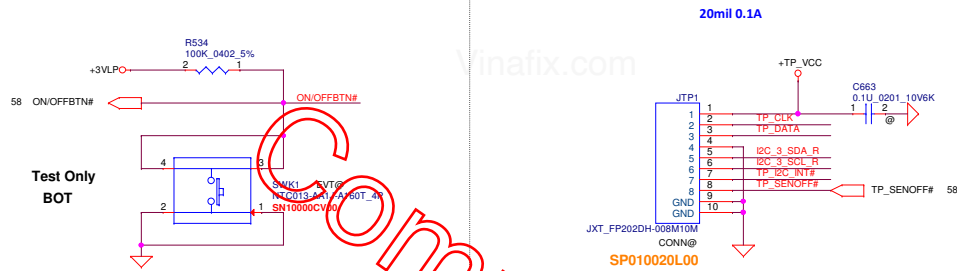


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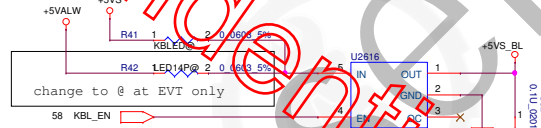
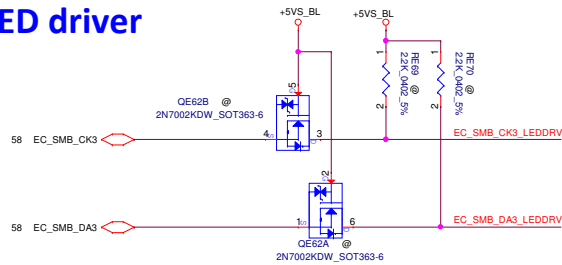
ON/OFF BTN

TP/B Conn.

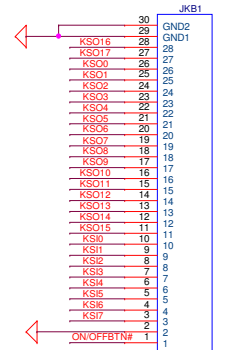
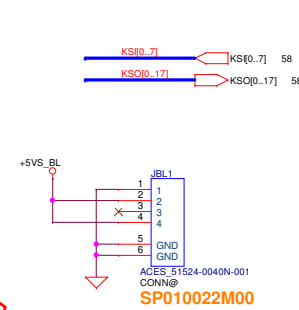


To EC
To APU

LED driver



KB Conn. / Backlight



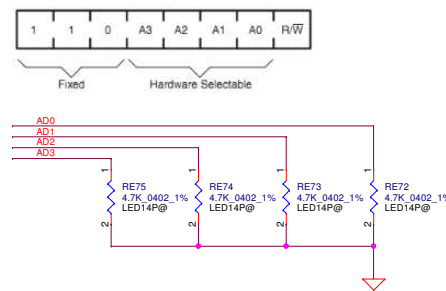
ACES_85201-2805

CONN@

SP01000GO00

set RE7 to 10k / output = 1.875mA

Raptor: NC for 59116F



KB Conn.
KB BackLight

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				Customer	FH50P M/B LA-H901P
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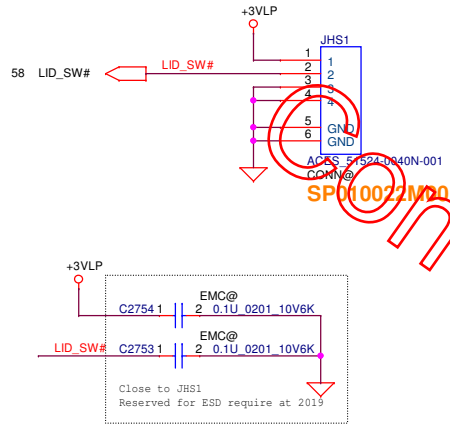
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				Size	Document Number	Rev
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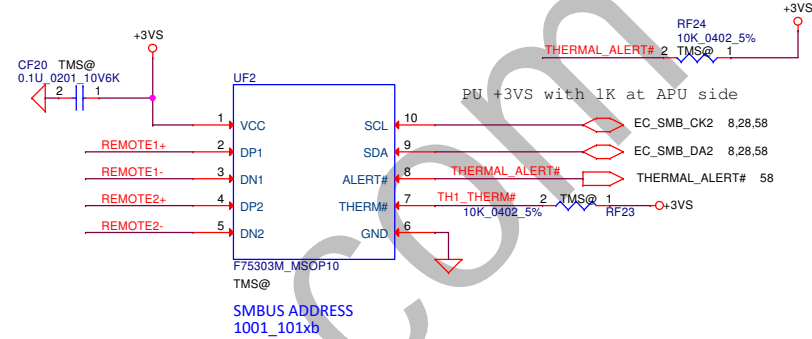
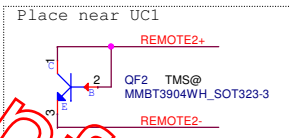
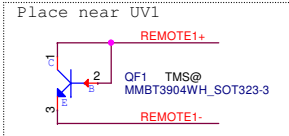
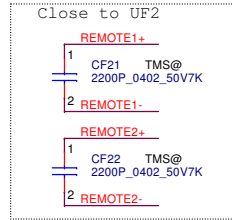
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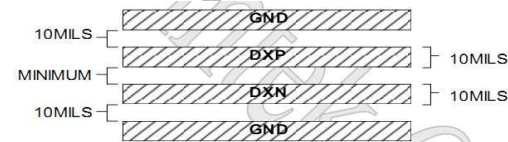
To Hall sensor/B



THERMAL SENSOR

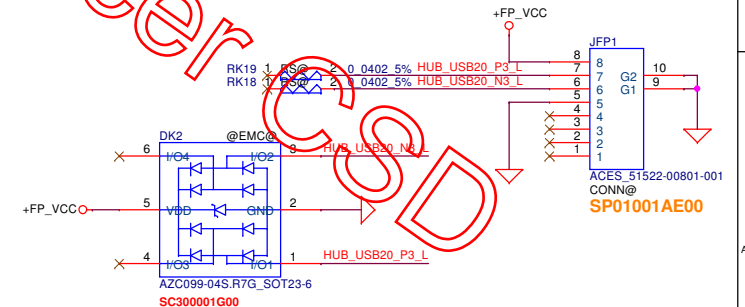
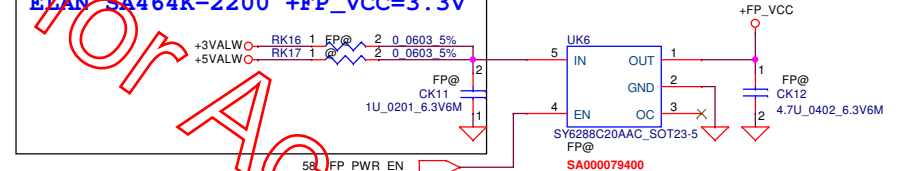


REMOTE1, 2 (+/-):
Trace length: <8"



Finger Print

Power Source Check
EG19 ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



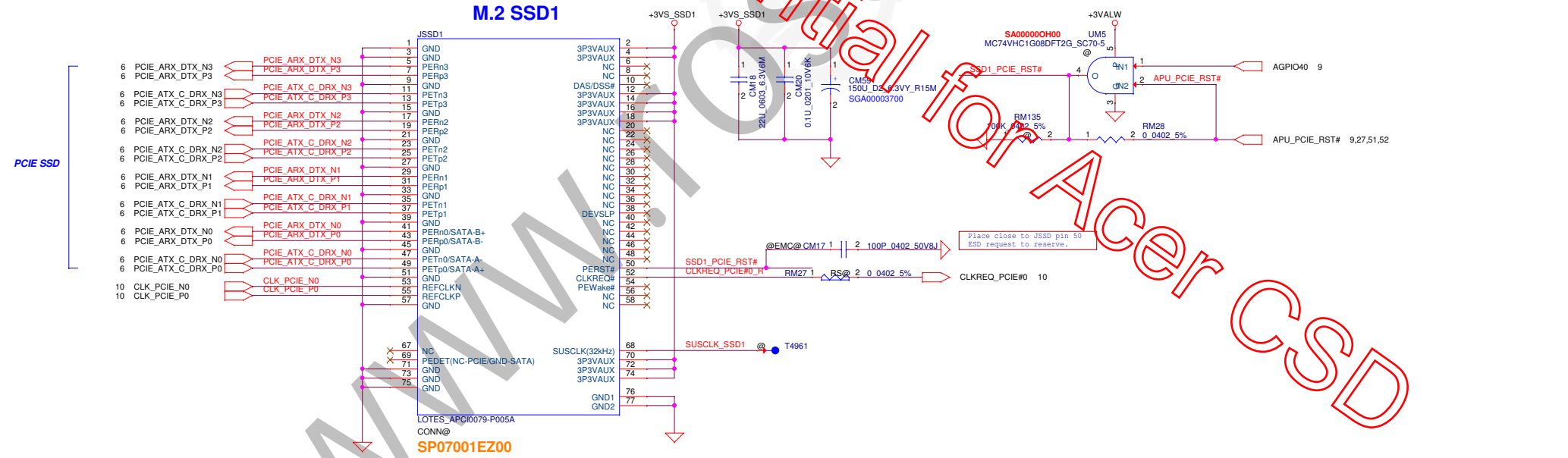
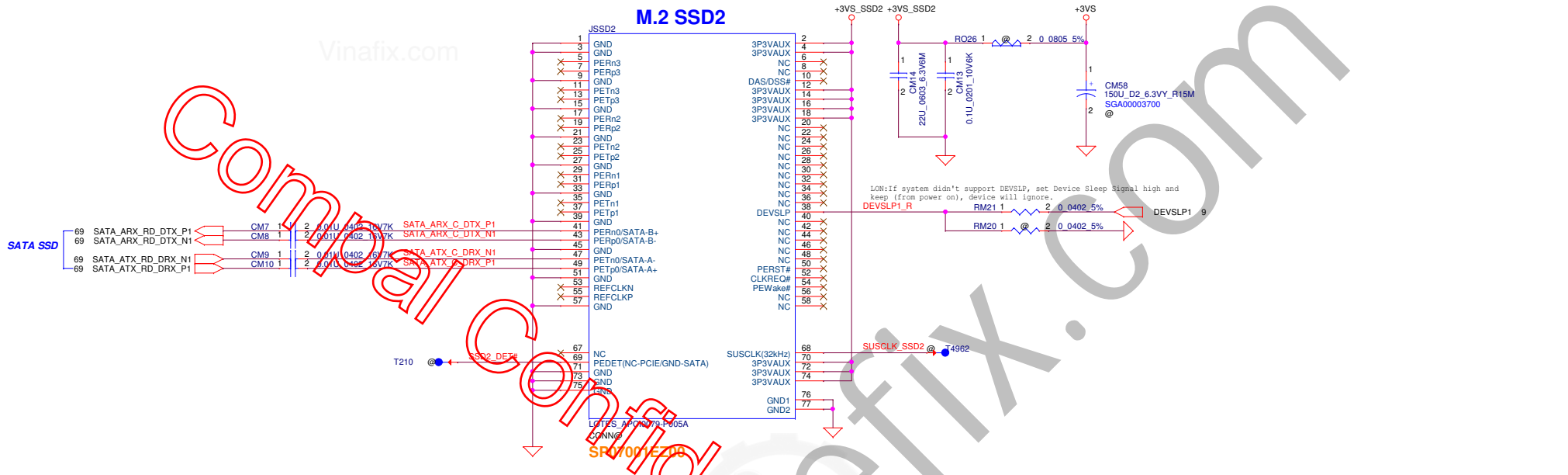
PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

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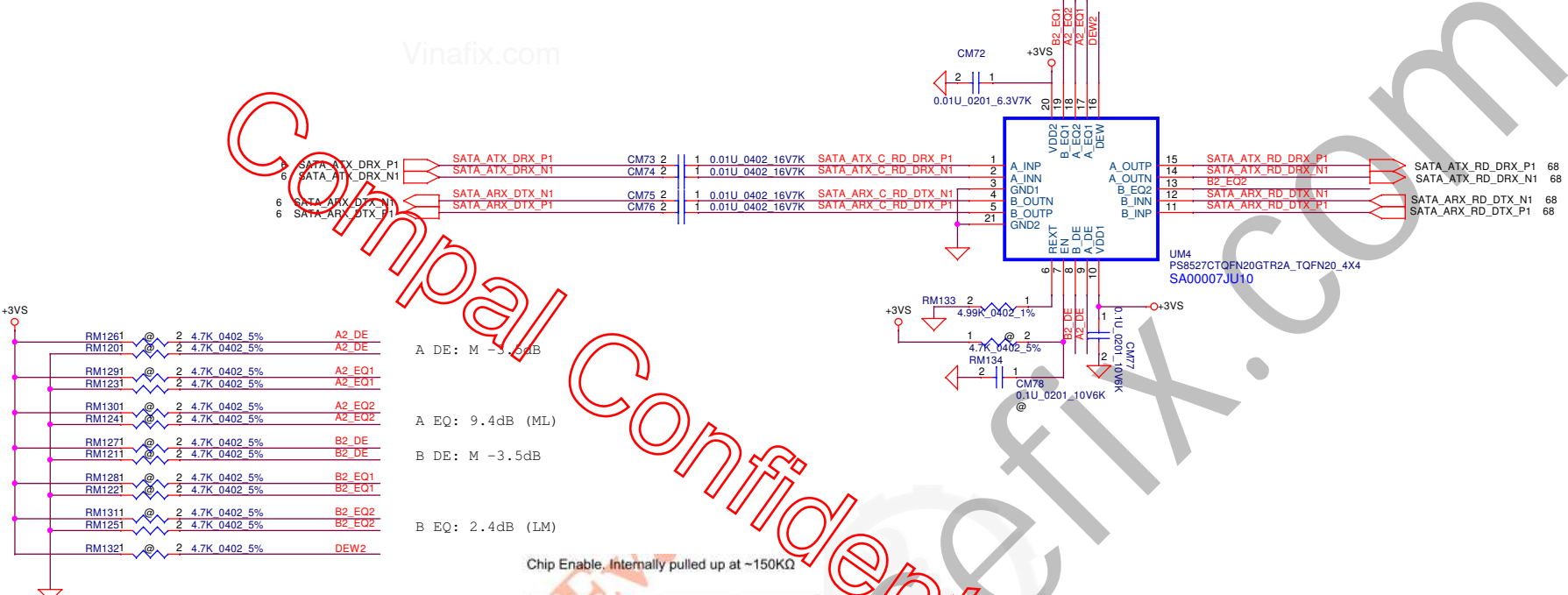


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SATA SSD Conn.



SATA Re-Driver for M.2 Connector



Chip Enable, internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_EmpHASIS
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_EmpHASIS
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

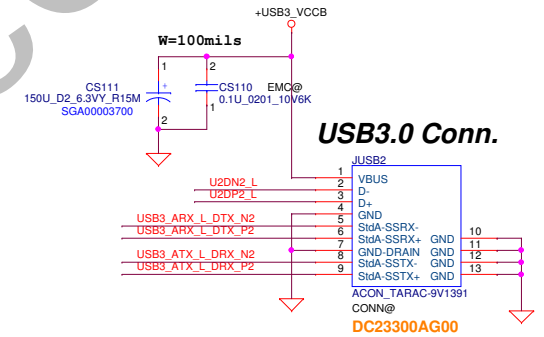
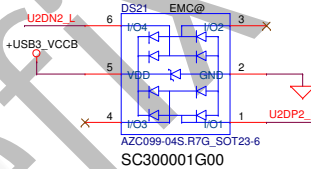
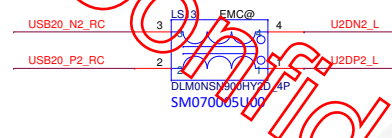
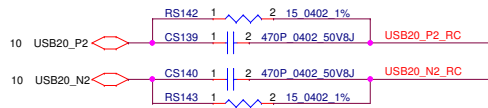
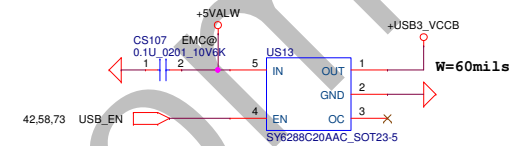
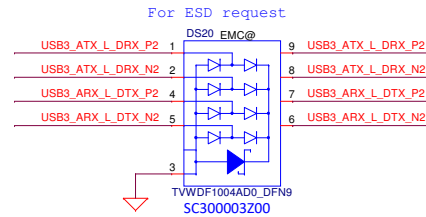
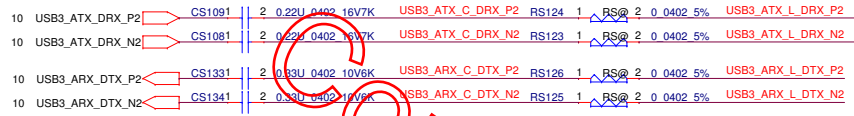
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

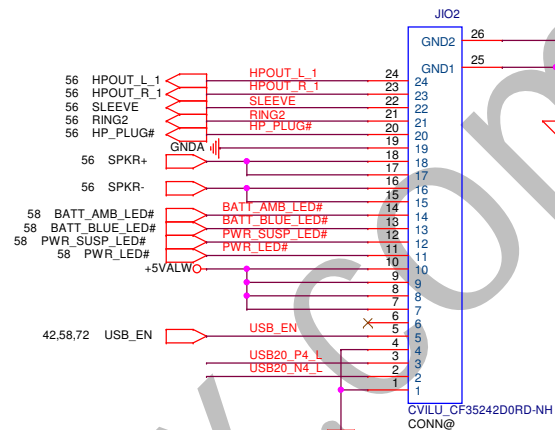
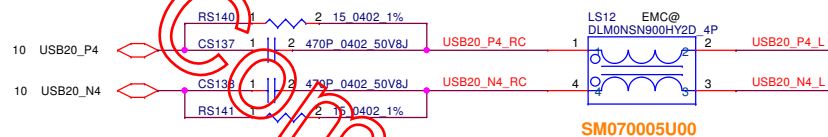
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IO/B CONN



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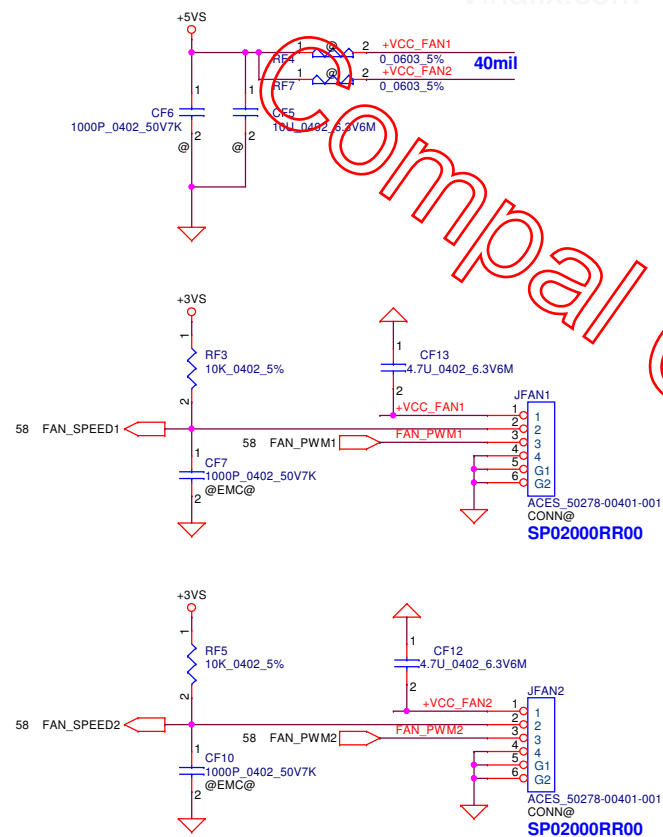
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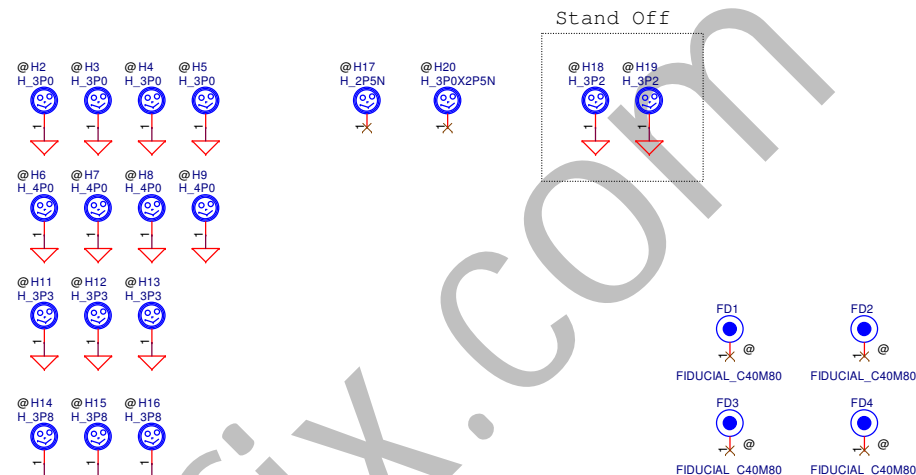
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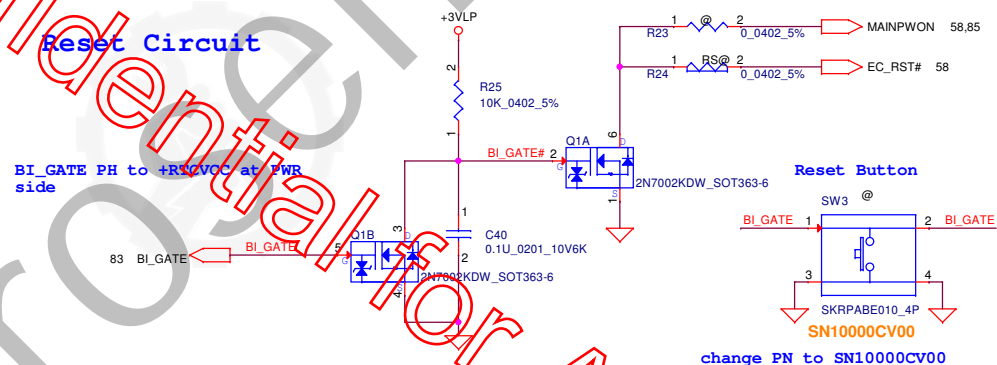
FAN Conn



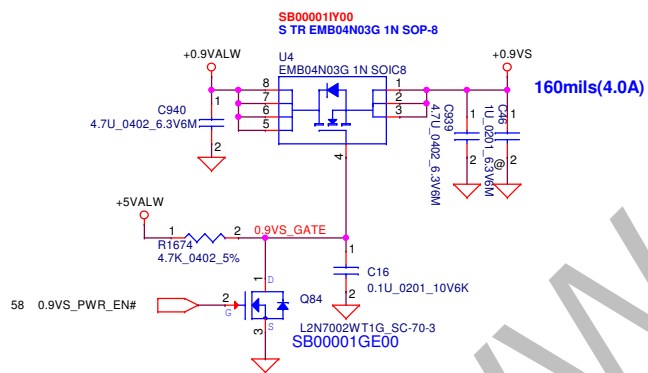
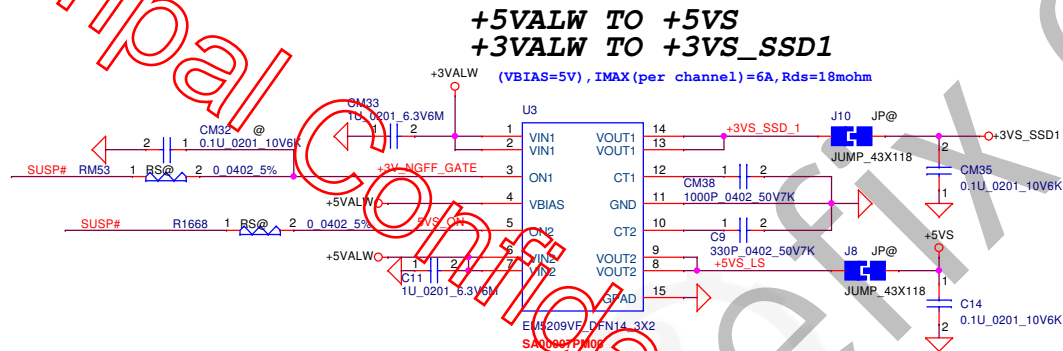
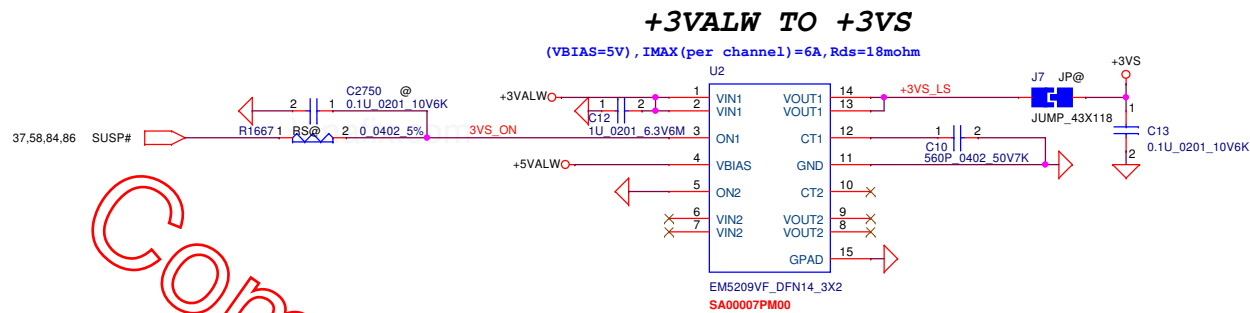
Screw Hole



~~Reset Circuit~~



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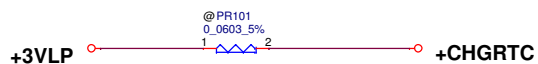
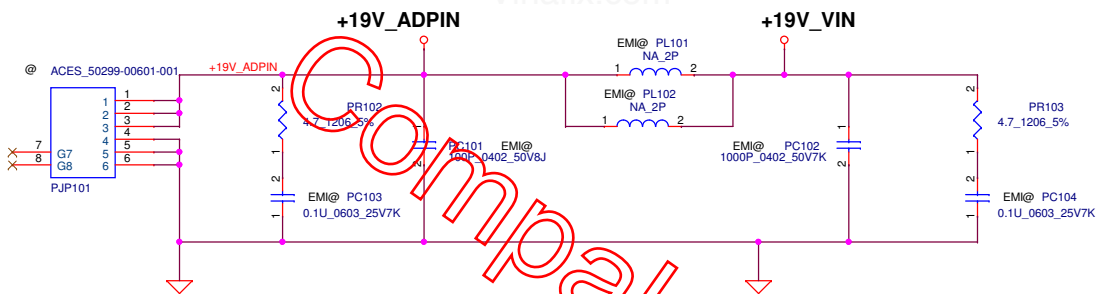
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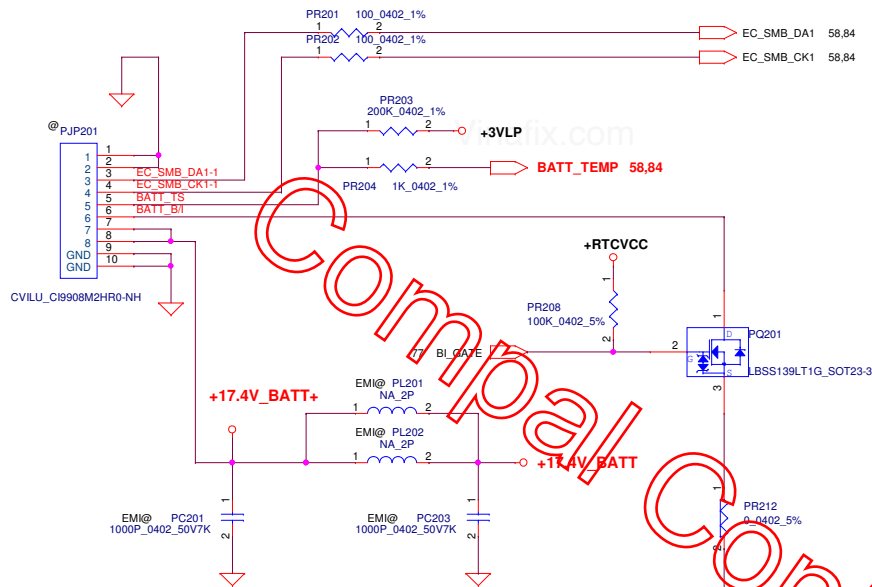
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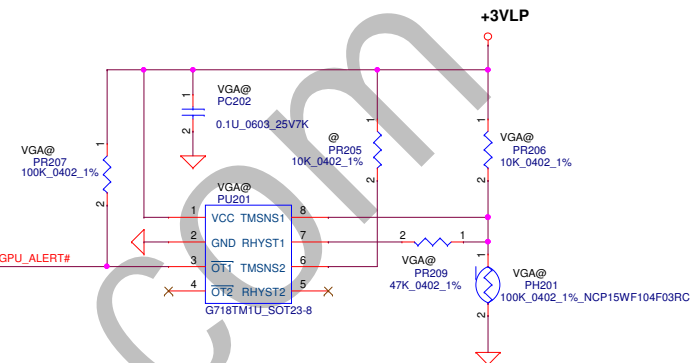
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58 GPU_ALERT#



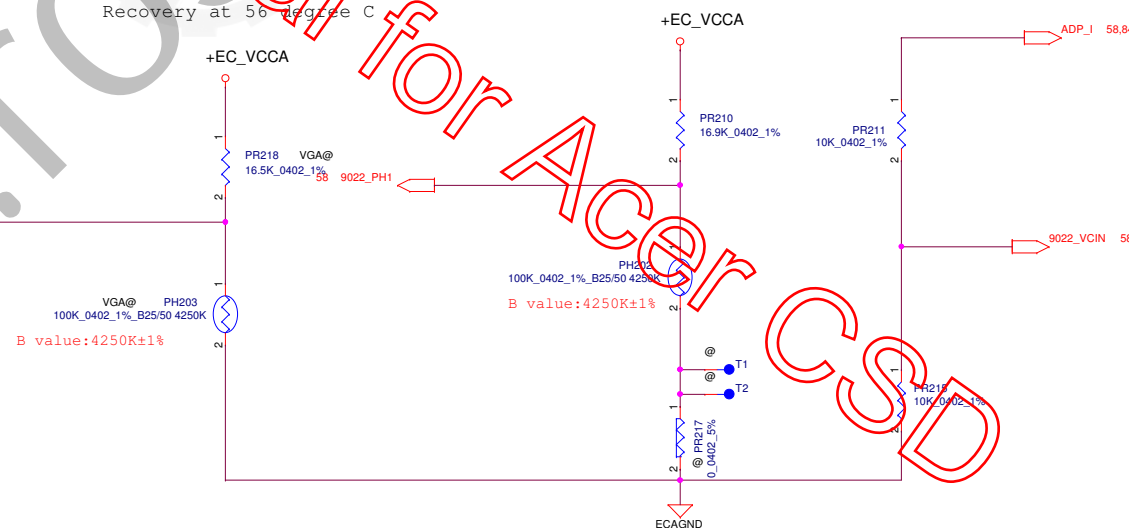
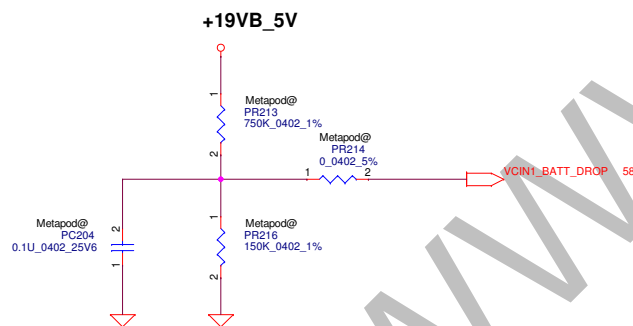
For KB9022 OTP	Active	Recovery
VCIN0_BH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

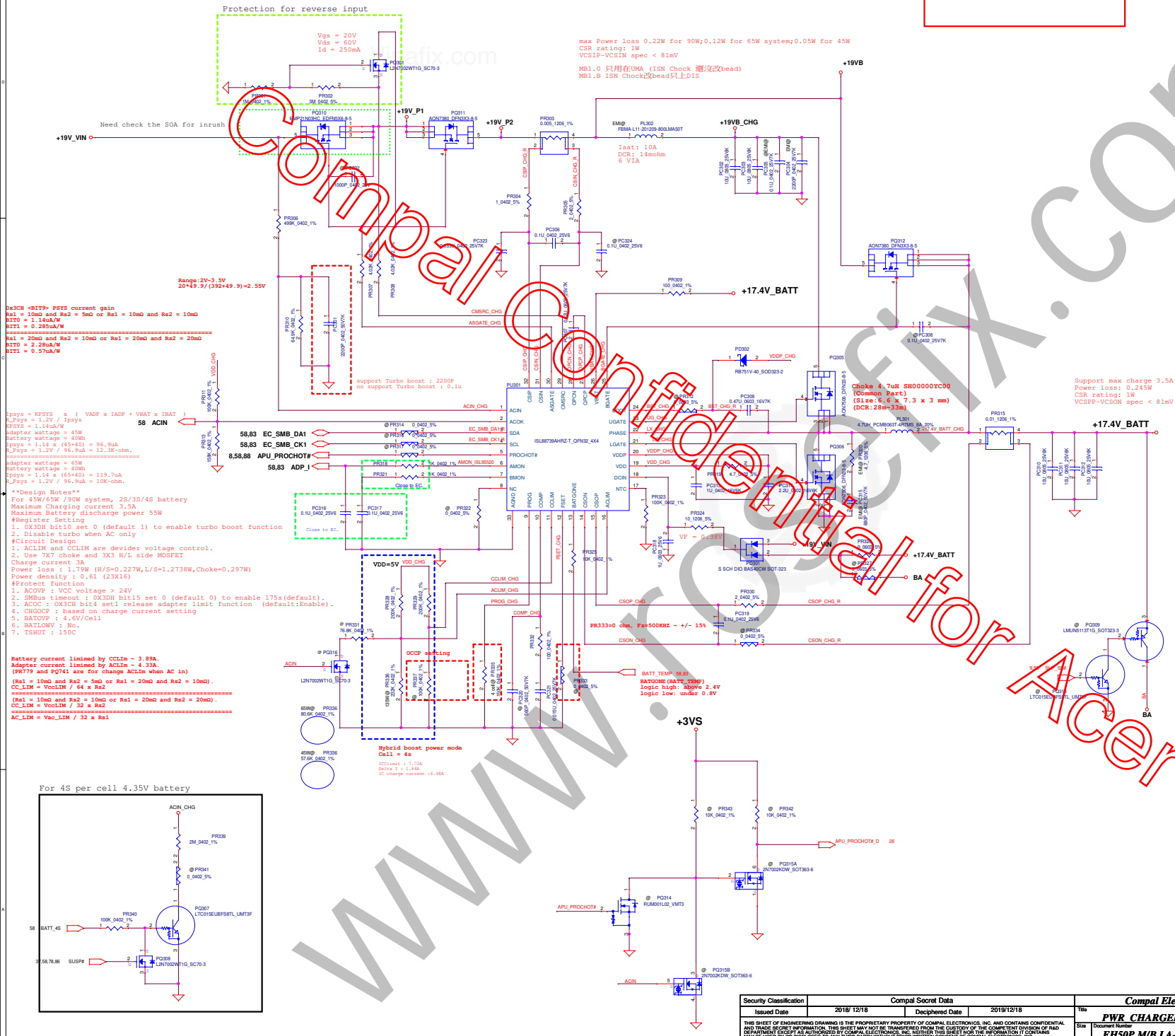
PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C

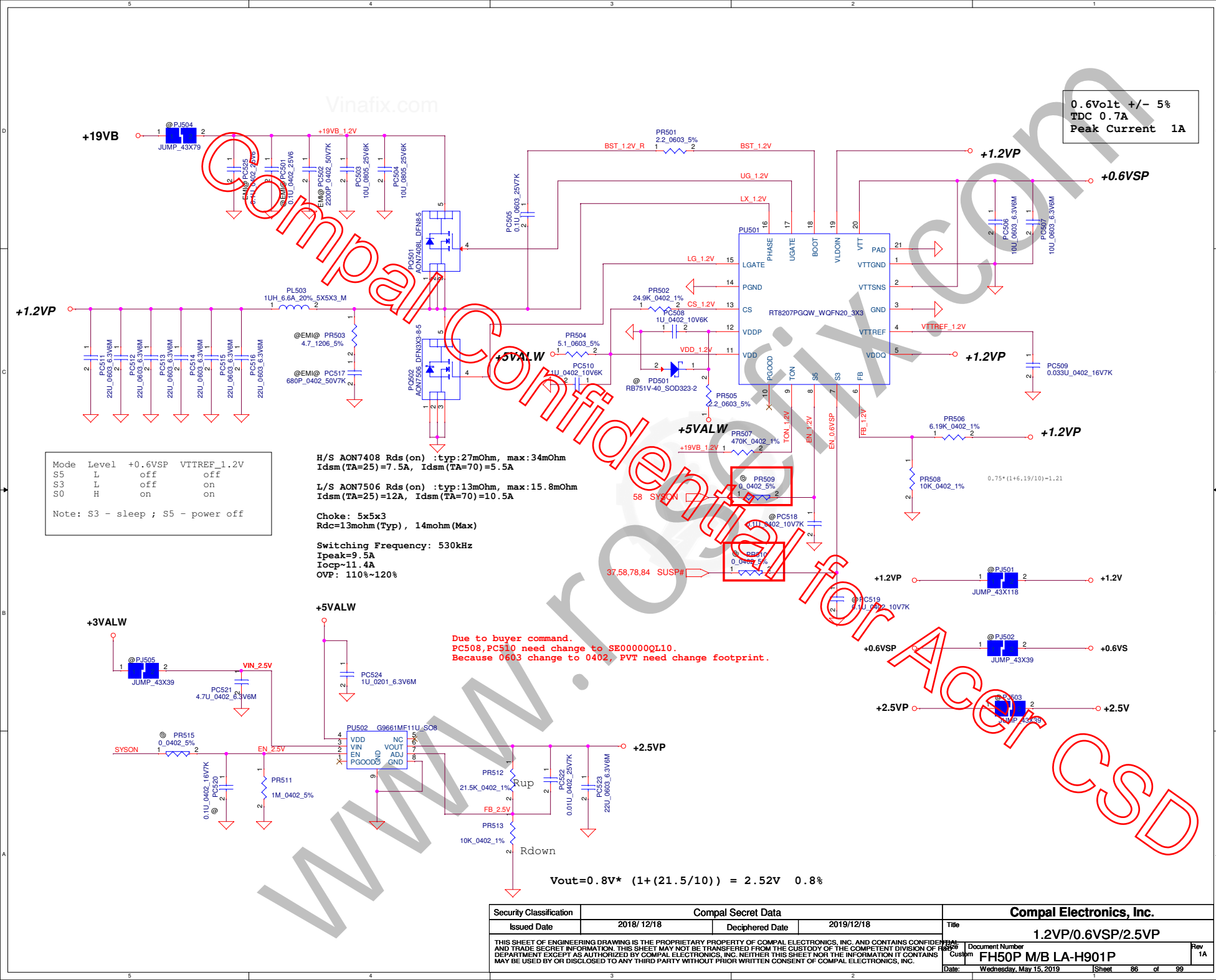
2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design

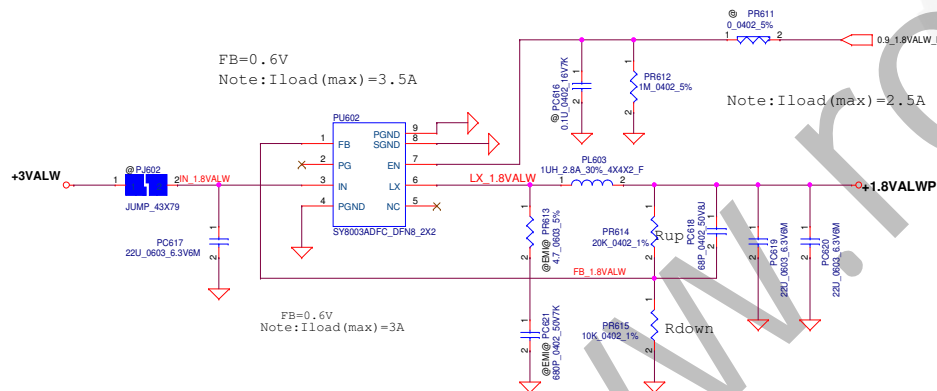
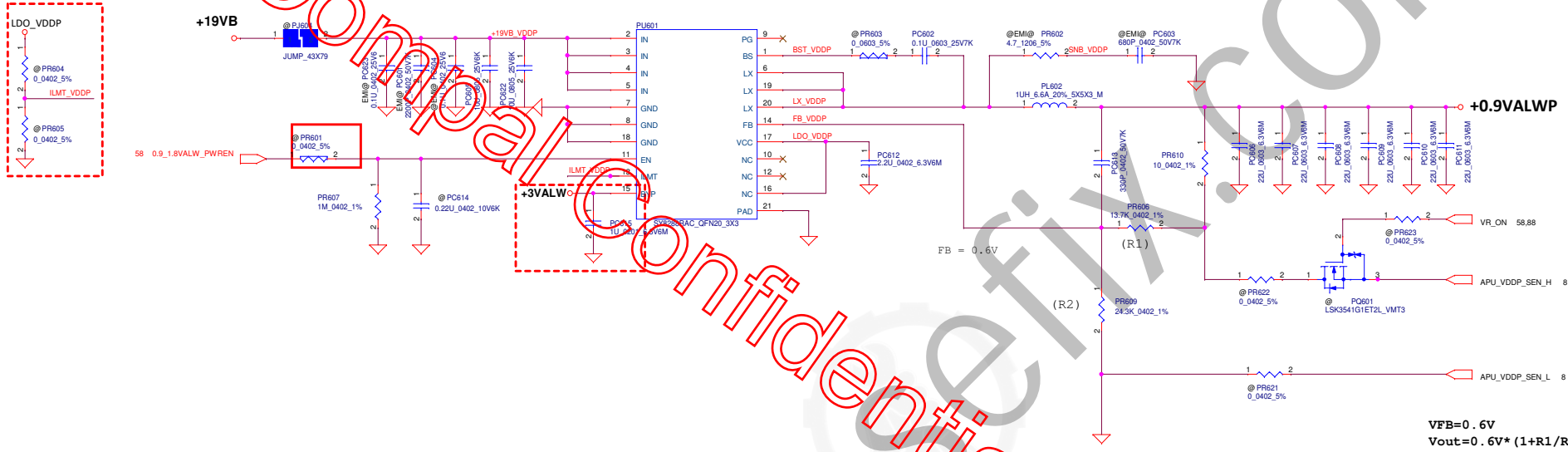


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								Size		Document Number		Rev	
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

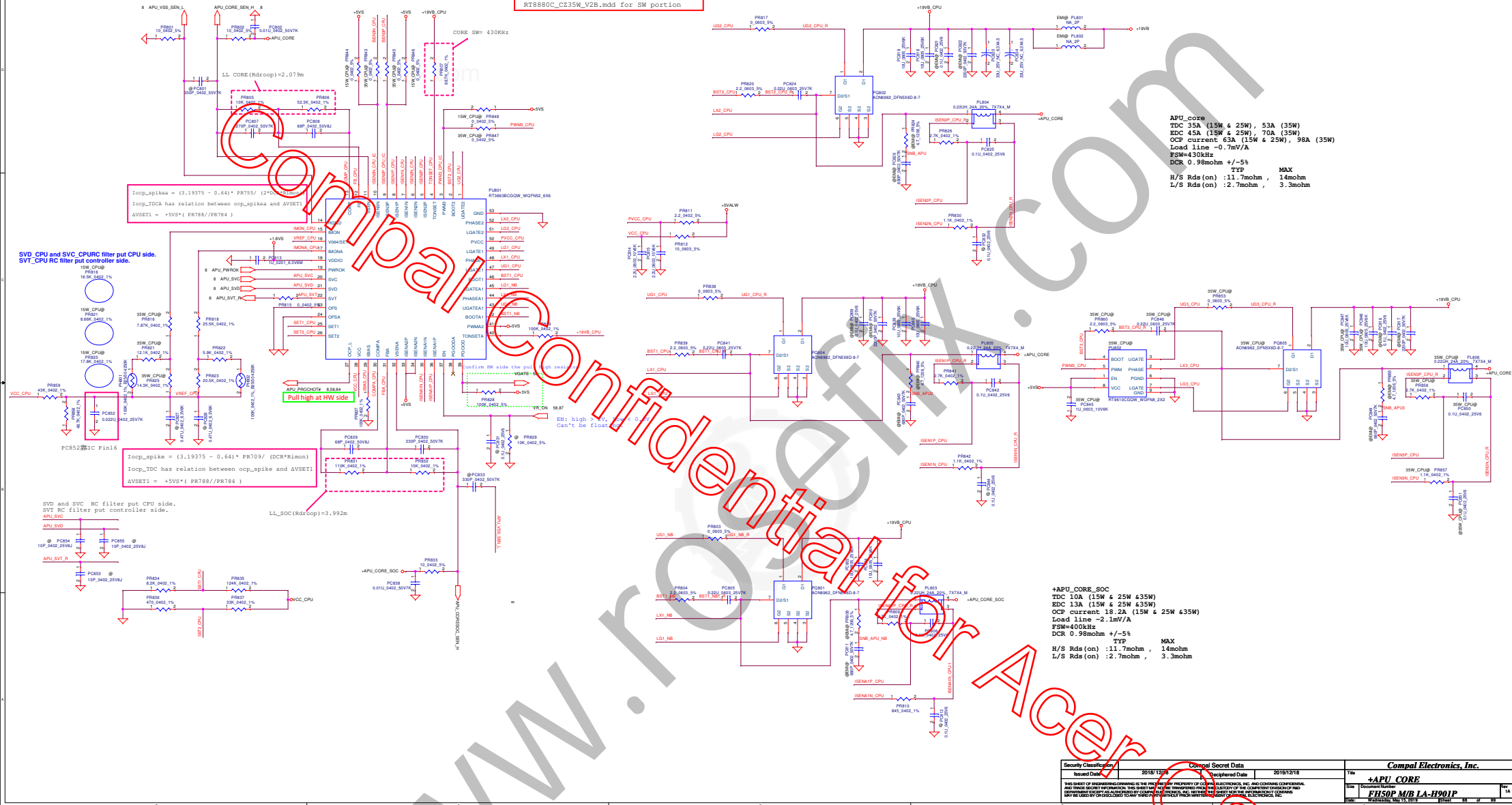


Note:
When design $V_{in}=5V$, please stuff snubber
to prevent V_{in} damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Module model information
RT8880C_CZ35W_V2A.mdd for IC portion
RT8880C_CZ35W_V2B.mdd for SW portion

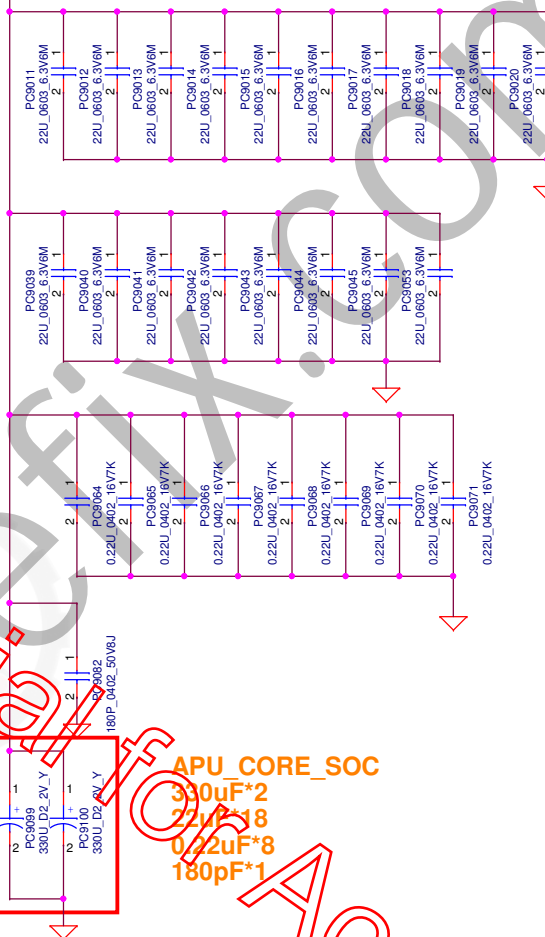


Security Classification		Control Secret Data		Control Secret Data	
Issued Date		2018/12/18		2019/12/18	
Revised Date					
Title		+APU CORE			
Size		1A			
Document Name		FH50P MB LA-H901P			
Rev		1.0			

Reserve Page

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+APU_CORE_SOC



near CPU

330u is common part SGA00009S00

APU CORE SOC

$$330\mu F \cdot 2 =$$

22uF*18

0.22uF*8

 $180\text{pF} \times 1$

APU CORE

330uF*5

22uF*27

0.22 μ F*8

180pF*1

330u is common part SGA00009S00

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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title +APU_CORE Cap	
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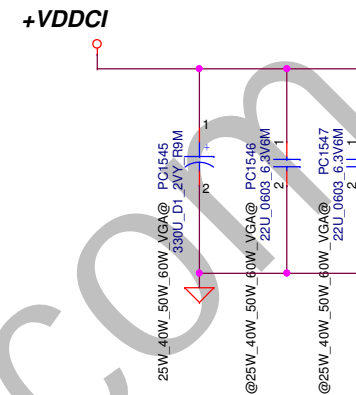
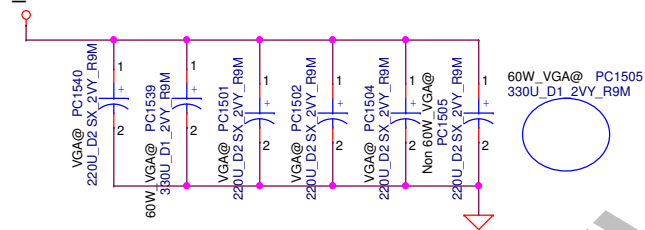
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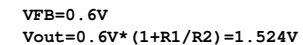
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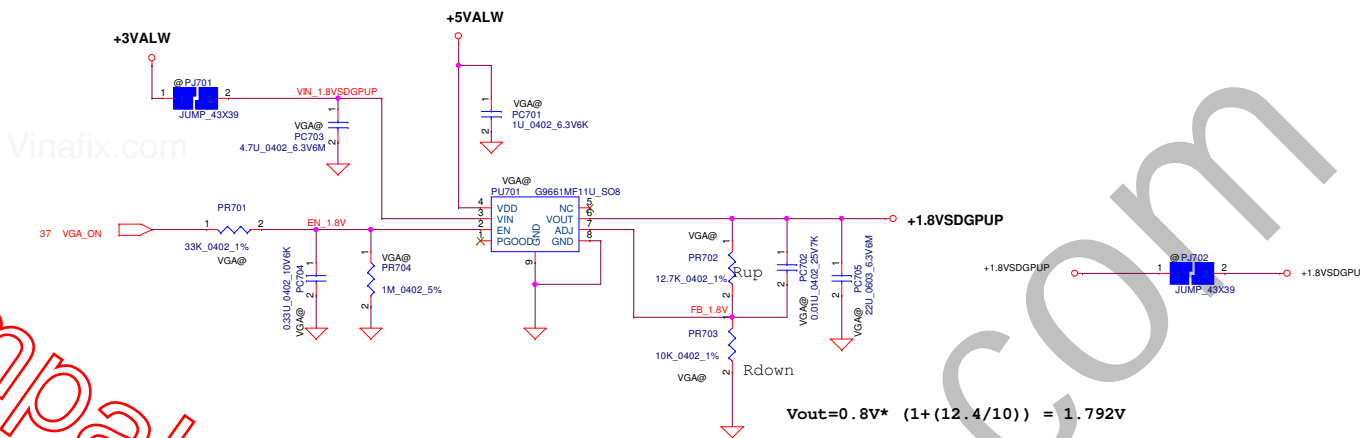
Module model information
SY8208D_V1.mdd



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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$$V_{out} = 0.8V * (1 + (12.4/10)) = 1.792V$$
$$V_{out} = 0.8V * (1 + (12.7/10)) = 1.816V$$
$$V_{out} = 0.8V * (1 + (13/10)) = 1.84V$$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	POWER Module design Change	0.1		PQ310: EMB04N03H_SB00001C500 -> _EMP21N03HC_SB00001LC00 PC313: 1U_0402_10V6K_SE00000QLT0 -> _1U_16V_K_X5R_0402_SE00000OU00 PC314: 1U_0402_10V6K_SE00000QLT0 -> _2.2U_16V_K_X5R_0402_SE000013780	2019/03/22	A
02	Design Update	CPU_CORE transient and load line test	0.1		PC830: 270P_0402_50V7K_SE074271K80 -> _330P_0402_50V7K_SE074331K80 PR831: 97.6K_0402_1%_SD034976280 -> _110K_0402_1%_SD034110380 Pr806: 34.8K_0402_1%_SD034348280 -> _52.3K_0402_1%_SD034523280 PC9097: 330U_D2_2V_Y_SGA00009S00 -> _Unpop	2019/03/22	A
04	Design Update	reduce part count	0.1		PR212: 0_0402_5%_SD028000080 -> _R-SHORT PR333: 0_0402_5%_SD028000080 -> _R-SHORT PR314: 0_0402_5%_SD028000080 -> _R-SHORT PR316: 0_0402_5%_SD028000080 -> _R-SHORT PR317: 0_0402_5%_SD028000080 -> _R-SHORT	2019/03/22	A
05	Design Update	reduce part count	0.1		Del colay PJ1401 PJ1402 PJ1403	2019/03/22	A
06	Design Update	prochot 調整	0.3		PR304: change R-SHORT SD028000080 0_0402_5% -> SD028100B80 1_0402_5% PC323: add NA -> SE000006O00 0.033U_0402_25V7K PC324: add NA -> @ SE00000G880 0.1U_0402_25V6 PR211: change SD034200280 20K_0402_1% -> SD034100280 10K_0402_1% PR310: change SD034665280 66.5K_0402_1% -> SD034649280 64.9K_0402_1%	2019/04/26	C
07	Design Update	EMI 需求	0.3		PR1437,PR1419,PR1402,PR1463: unpop ->SD001470B804.7_1206_5% PC1412,PC1426,PC1408,PC1467: unpop ->SE074681K80680P_0402_50V7K	2019/05/07	C
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Size	Customer	Drawn Number	Rev
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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				1A	1A

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1			03/28	Change 0 ohm to R-Short	R1667, R1669, RM53, RX21 change to R-Short	PVT	1.0
2	10	CPU	03/28	ESPI_ALERT_L PU to VDD	Add RC6168 and PU to +3VS	PVT	1.0
3	29	CLK GEN	03/28	27MHz Crystal Correlation Update	CV450, CV451 change to 15P_0402	PVT	1.0
4	38	Panel	03/28	144Hz Panel OD Function Circuit Update	Rename PANEL_OD_EN to PANEL_OD# UN-POP RX11	PVT	1.0
5	40	HDMI	03/28	Mask un-use co-lay component	L2512, L2513, L2514, L2515 footprint change to INPAQ_HCM1012GH900BP_4P-NPM	PVT	1.0
6	43	TypeC	03/28	TypeC current limiting adjust	RS109 change to 4.3K_0402 RS110 change to 8.2K_0402	PVT	1.0
7	51	LAN	03/28	Contact YL1 Value Change DL1 Material	YL1 update vale to XRCGB25M000F2P34R0 DL1 change from SCA00002M00 to SCA00001A00	PVT	1.0
8	68	M.2 SSD1	03/28	Reserved Circuit for PCIe compatibility	Change RM28 to 0_0402 Add RM135, UM5	PVT	1.0
		M.2 SSD2	03/28	BOM change M.2 SSD2 power need a break point	Pop RM21, un-pop RM20, CM58 Add RO26, JSSD2 power change to +3VS_SSD2		
9	75	HUB	03/28	BOM change	Change RS154, RS152 with HUB@	PVT	1.0
10	77	Others	03/28	Screw hole change	H11, H12, H13 change from H_3P8 to H_3P3	PVT	1.0
11	78	DC-DC	03/28	Material Change	U4 change to SB00001TY00	PVT	1.0
12	06	CPU	03/29	Add R5/ R7 CPU PN	Add SA00000CR600 SA00000C7680	PVT	1.0
13	06	CPU	04/01	Material Change	YC2 Change from SJ10000AF00 to SJ10000JP00	PVT	1.0
14	09	CPU	04/02	BOM change	Un-Pop RC693	PVT	1.0
15	10	CPU	04/02	BOM change	YC3 change to SJ10000PW00 CC686 change to 12P_0402 CC682 change to 10P_0402	PVT	1.0
16	28, 38, 58, 63		04/02	Material Change	DV1, DV2, DV4, DX2, D2012, D2013, D2014, D22 change to SCS00009P00	PVT	1.0
17	58	EC	04/26	Add Board ID for MP	Add R1564 15K_0402_1% for MP	MP	1A
18	75 52 38 66 58	HUB	04/30	Remove Hub and other component/net	Delete RS148 ~ RS158, CS145 ~ CS153, YS1 US15 Move RS146, RS147, CS143, CS144 to page52 and POP Delete net HUB_USB20_P2/HUB_USB20_N2 (JEDP1 pin 29/30) Delete net HUB_USB20_P3/HUB_USB20_N3 (RK19, RK18 pin 1) Delete net USB_HUB_RESET# (U44 pin 126)	MP	1A
19	52	M.2 SSD1	04/30	Reserved 10U_0603 on WLAN Power	Reserved CM79, CM80	MP	1A
20	52	M.2 SSD2	05/14	WLAN power path change	Un-Pop RM101 POP UM3, CM71	MP	1A
21	37	DC-DC	05/14	Adjust C21 for +1.8VS Sequence	Change C21 to 4700pF	MP	1A

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